MANUAL
MANUAL
MANUAL
MANUAL

Maintenance Manual

Compucolor® Corporation

P.O. Box 569
Norcross, Georgia 30071
Telephone 404/449-5996

Compucolor®

II

Maintenance Manual

ISC 216 - 978 - 999208

PROPRIETARY STATEMENT

TABLE OF CONTENTS

VIII Drawings

NOTE: See Section VII for Assembly Part Numbers. PCB Numbers shown above refer to bare PCB only.

SECTION I
COMPUCOLOR II SPECIFICATIONS

I. SPECIFICATIONS

Operating Conditions

Power	105-125 Volts, 50/60 HZ., 150 Watts
Temperature	+ 10° C to + 40° C Operating - 30° C to + 70° C for storage only
Humidity	0 to 95% non-condensing

Physical Dimensions

Cabinet	18.0" W x 13.6" H x 15.8" D
Keyboard	18.7" W x 2.8" H x 6.9" D
Weight	37 pounds, including keyboard
Shipping Weight	45 pounds complete
Screen Size	13 inch diagonal, 90 square inches in area Display normally uses 60 to 70 square inches.

Performance

CRT Display	Eight colors, background and foreground (red,green,blue,magenta,cyan,yellow,white and black)
	64 Characters per line 32 lines per page, or 16 lines with 2X character height
	64 ASCII characters, 5 x 7 dot matrix within a 6 x 8 dot pattern, plus 64 special characters in a 6 x 8 matrix. Expandable to include graphics of 128 x 128 and vector generating software. Cursor is white blinking over-score and underscore, non-destructive.
Keyboard	Standard ASCII 4 level, coded with 192 codes. 72 gold crossbar commercial key switches. CPU Reset and Automatic disk loading in-cluded. Optional 101-key and 117-key units include color, numeric and function keys.

Microcomputer	Central Processing Unit, 8080, 2 microsecond CPU with total memory expandable to 64K bytes
	Read Only Memory (ROM): 16K bytes of non-destructive read only. Memory sockets included for 12K bytes of additional EPROM/MROM memory. Includes DISK BASIC 8001, File Control System, and Terminal Software.
	Random Access Memory (RAM): 4K bytes for screen refresh. 4K bytes for user workspace. Room for 28K bytes of additional user workspace.
	Input/Output Ports: System is designed for 512 ports, with 25 ports implemented in standard unit. Optional: one RS-232C Serial Asynchronous Channel for a printer or modem.
	Editing: Page/Roll Mode, Erase line, Erase Page, Tab, Caps Lock, CPU Reset, and Color Selection.
	Language: DISK BASIC 8001 interpreter in ROM memory includes: 27 statement types: CLEAR, DATA, DEF, DIM, END, FILE, FOR, GET, GOSUB, GOTO, IF, INPUT, NEXT, ON, OUT, PLOT, POKE, PRINT, PUT, READ, REM, RETURN, RESTORE, STEP, THEN, TO and WAIT. 5 command types: CONT, LIST, LOAD, RUN and SAVE. 18 mathematical functions: ABS(x), ATN(x), CALL(x), COS(x), EXP(x), FRE(x), INT(x), INP(x), LOG(x), PEEK(x), POS(x), RND(x), SGN(x), SIN(x), SPC(x), SQR(x), TAB(x) and TAN(x). 9 string functions: ASC(x$), CHR$(x), FRE(x$), LEFT$(x$,I), LEN(x$), MID$(x$,I,J), RIGHT$(x$,I), STR$(x) and VAL(x$). Disk File commands: COPY, DEVICE, DIRECTORY, INITIALIZE, LOAD, PRINT, READ, RENAME, RUN, SAVE and WRITE.
	Baud Rate: Independent Baud Rate generators for one of 7 Baud rates from 110 Baud to 9.6K Baud.

Disk Drive	Uses 5.25" diskette. Tracks: 40 Track Density: 48tpi Access Time: average (40 tracks): 400ms Average Latency: 200ms Transfer Rate: 76.8 Kilobits/sec. Performance specifications: Capacity formatted 51.2K Bytes/Side. Both sides usable by flipping diskette over.

SECTION II
COMPUCOLOR II INSTALLATION

II. INSTALLATION

Compucolor II is intended for use on a desk or table or any similar vibration free horizontal surface that is free from lint and dust. (However, it is best to avoid metal top desks and the vicinity of large metal objects. Their presence may interfere with proper disk drive performance.) It may be used under normal room lighting conditions, although slightly subdued lighting will improve the display appearance (as for a color television set). The Keyboard is usually placed in front of the CRT screen, with the flat, flexible cable running beneath the console to J1 of the Logic Board, accessible through the rear cover. (Note that terminal 2 of the plug goes up). A space 19 inches wide by 24 inches deep is adequate. If the optional additional Disk Drive is used, it may be placed alongside the console (increasing space width by 6 inches) or in some other location within reach of the connecting cable. While no special cooling provisions need be made for Compucolor II, there must be free flow of air around the console--do not place anything on the cabinet that will restrict air flow.

Compucolor II may be used adjacent to most types of electrical equipment and appliances provided it is not within a strong magnetic field. (Operation within a strong magnetic field may disturb operation of the display and transfer of data to or from the diskette).

Unless used with a modem connection to a telephone line, the only external connection is the 6-foot 3 wire power cord to 115VAC power. If connection is to be made to an RS-232 compatible modem, the user provides the necessary cabling. The cable between the Compucolor II and the modem should not exceed 50 feet in length. The terminals on connector J2 at the rear edge of the Logic Board are shown in the table below. The usual modem connections are indicated; however, the modem manufacturer's instructions should be consulted.

LOGIC BOARD J2 TERM. NO.	MODEM TERM. NO.	SIGNAL
1	1	AA - Protective Ground
3	2	BA - Transmitted Data
5	3	BB - Received Data
7	4	CA - Request to Send
14	7	AB - Signal Ground
15	20	CD - Data Terminal Ready

For a quick check procedure, see "Operational Test" in the MAINTENANCE section (following "ALIGNMENT").

To connect the external Add-on Disk Drive (optional), first disconnect the keyboard cable from the Logic Board. Then connect the add-on drive's cable to the Logic Board's J1 (terminal 2 of the plug up). Now connect the Keyboard cable to the additional connector on the Disk Drive cable (near the Logic Board end).

For information regarding add-on RAM or ROM, see Section V, SUBASSEMBLY DESCRIPTIONS (near end of section).

SECTION III
COMPUCOLOR II OPERATION

Compucolor® II Instruction Manual

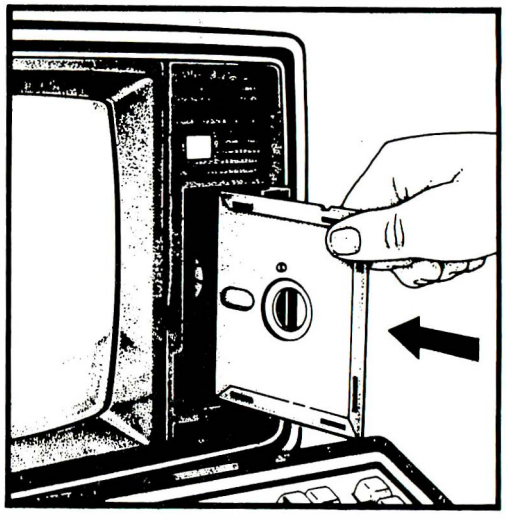
The Compucolor Corporation thanks you for purchasing a Compucolor II. Although many precautions have been taken to assure that this material is received in good condition, we ask that you take a few minutes to read the following material so that you may derive maximum enjoyment and use from your Compucolor II.

The handbook has been divided into six sections. Section One gives directions for operating the Compucolor II and describes a step by step procedure for loading a program into the Compucolor II from a diskette. Section Two describes the keyboard and tells you how to write and expand a simple program. Section Three summarizes BASIC and various FCS and CRT commands. Section Four concerns handling and care of diskettes as well as other precautions. Section Five lists a variety of books on the market that deal with computers and programming. Section Six provides lists of port assignments, memory locations, the fifty pin bus and RS232C Interface, as well as a complete character set.

Contents

Section I
How to operate the Compucolor II

1. Place the Compucolor II in a convenient location remembering that you will probably enjoy sitting and playing games on the computer for hours at a time. Be careful not to obstruct the air flow through the vent on the back of the unit.
2. Now connect the keyboard cable to the socket labeled "Keyboard" on the back of the Compucolor II. This connector will only fit one way, so if it doesn't fit, turn it over and try pushing in without forcing it. Find the CAPS LOCK key to the left of the space bar on the keyboard. Make sure this key is in the down position (see page 4).
3. Next plug the power cord into the back of the computer much like you would plug in an electric frying pan. Then plug the other end of the power cord into the wall socket. You may need an adapter if your socket cannot take a three-prong insert.
4. It's now time to turn on the Compucolor II by pushing to one side the "Power" (white) button on the back of the unit, just above the cord.
5. The Compucolor II will require 60 seconds for the tube to warm up before the message "DISK BASIC 8001 V6.78 COPYRIGHT© BY COMPUCOLOR" will appear.
6. If it does not appear then hold the SHIFT and CONTROL keys down and press the CPU RESET key. (Note: leave the SHIFT and CONTROL keys down for at least 5 seconds after pressing CPU RESET key.)
7. Take the diskette that came with your Compucolor II and slip it into the right side of the computer. Make sure the diskette is inserted correctly and then close the door. See illustration.



8. Push AUTO (brown key in upper left hand corner).
9. You will see a list or "MENU" of programs on the screen. Select the program by the number at left. Type in the number and press the ENTER key.
10. The program you selected will be loaded into the Compucolor II and you will see directions on the screen on how to proceed with the program you selected. Have fun.
11. If nothing appears on the screen after pressing AUTO key try turning the diskette over and follow the instructions starting at step 6.
12. If it still doesn't work after trying it again, then simply press the CPU RESET key with no other keys held down. The display will now say, "COMPUCOLOR II CRT MODE V6.78." If this does not appear turn the unit off for 15 seconds and then try from step 4.
13. After the "COMPUCOLOR II CRT MODE" message appears, press the (ESC) key and the (BASIC) or letter W key. The following message should appear: "DISK BASIC 8001 V6.78 COPYRIGHT © BY COMPUCOLOR." "MAXIMUM RAM AVAILABLE?" Now type "8192" and press the ENTER key. (If your Compucolor II is a Model 4 type "16384," then ENTER. If a Model 5, type "32768" then ENTER.) The unit will come back with the amount of free RAM memory available and the "READY" message. Now go to step 7. NOTE: if the ENTER key is pressed without entering a number the unit will search for the maximum RAM in your Compucolor II.
14. If the above does not provide the required results contact your local dealer for assistance, or call Compucolor Corporation's toll-free HOT LINE: (800) 241-4310.

Section II
Computer Basics

Compucolor II is a microcomputer. Housed within your Compucolor II is a single integrated circuit chip called a microprocessor. This is the very heart of your Compucolor II. The microprocessor is the computing device for storing programs and for performing logical operations. The microprocessor, called the Central Processing Unit, or CPU, controls all operations of the Compucolor II.

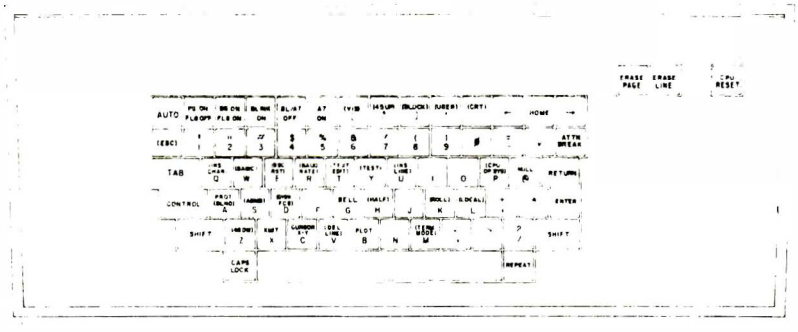
Compucolor II is capable of storing and filing information. Data is fed into the computer by means of typing on the keyboard. This process called INPUT uses the keyboard as its device. To view what has been fed into the computer, Compucolor II uses a display screen called a cathode-ray-tube or CRT display unit, to show OUTPUT.

As soon as your Compucolor II is turned on, you are ready to play games, program, store and retrieve information. You are in "DISK BASIC 8001." If you followed the instructions on page 2 of this manual you were able to load a diskette and run a program. Now we'd like to re-introduce you to your Compucolor II so that you can communicate with it effectively.

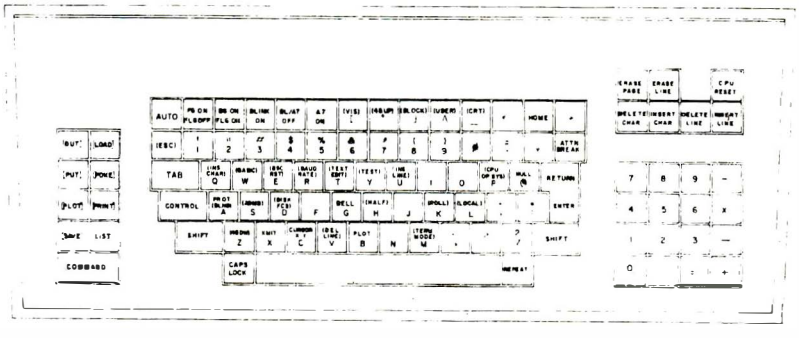
Compucolor II has within it a well defined set of rules for communicating with you. Your task is to learn what the computer already knows. Together, you and Compucolor II will communicate in such a way that Compucolor II will do as you say.

Communicating with Compucolor II means that you will be feeding data or information into your unit by means of a KEYBOARD. Let's take a few minutes to talk about some of the keyboard's features.

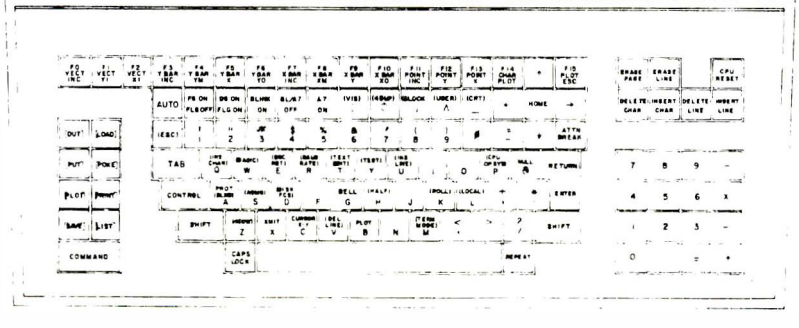
STANDARD



EXTENDED (Optional)



DELUXE (Optional)



Keyboard Operation

CAPS LOCK

Typing words on the Compucolor II is only done in capital letters. To facilitate the use of capitals, a CAPS LOCK key is used. Located on the left next to the space bar, the CAPS LOCK key will stay depressed and all letters typed will be capitals. By using the SHIFT key, special characters can be printed while the CAPS LOCK key remains depressed. To unlock the CAPS LOCK key, depress it once. The key is now flush with the space bar and special characters are now typed when the SHIFT key is not depressed. With the SHIFT key depressed capital letters are typed. The numbers and punctuation keys work the same as a regular typewriter. SHIFT gives the top character on a key and unshift gives the bottom character on a key.

SHIFT KEY

Compucolor II's keyboard is much like an ordinary keyboard with some additions. Like a regular typewriter, the SHIFT key is used to type upper case characters and in some cases, special characters. The SHIFT key must be depressed until the desired character is typed.

AUTO

The AUTO key on the upper left has been specially programmed so that when you press the AUTO key a program called "MENU.BAS" will be loaded from the diskette and caused to run. It will list on the screen all programs that can be run under the "MENU" system.

RETURN ENTER

The RETURN-ENTER key is on the right side of the keyboard. By pressing this key when you are in DISK BASIC you command the Compucolor II to accept the most recent instruction entered. If you are in the "CRT MODE" then this will only cause a carriage return as on a typewriter.

DIRECTION ARROWS, HOME

Three direction arrows and a HOME key are located on the right side of the keyboard. The HOME key and the arrow keys control the cursor. Pressing HOME brings the cursor to the upper left hand of the screen. The direction arrows are used for correcting typing mistakes or to carry you to another spot on the screen.

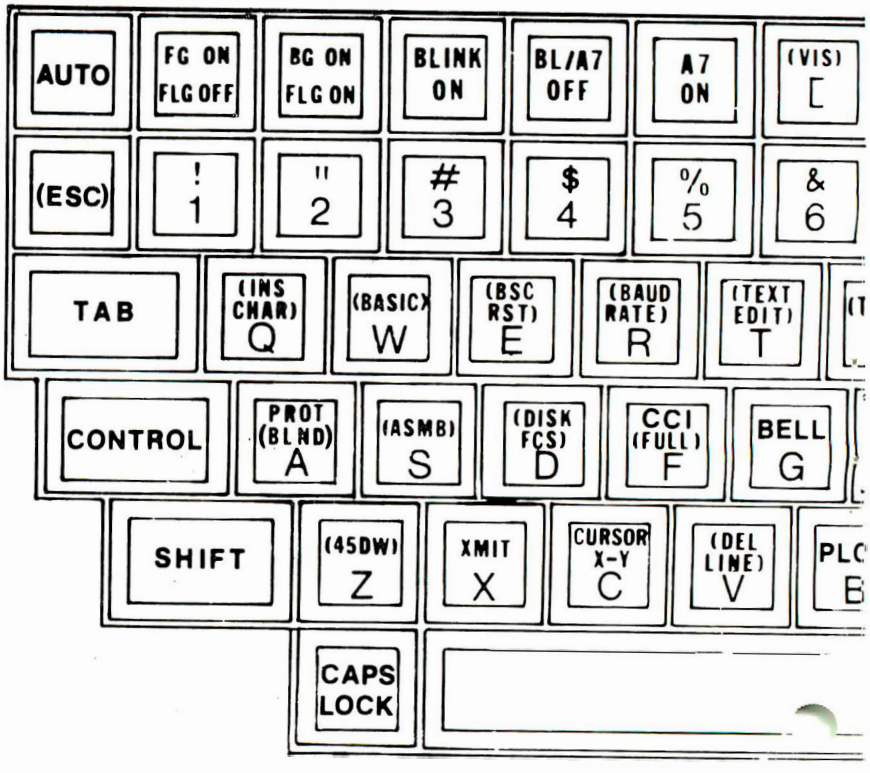
To correct a typing error in DISK BASIC press the ← arrow until you have erased the error. This backspace key erases all letters, one at a time, that it touches. For example, if you had typed "NOW IS THE TYME"←←←retype "IME."

The following keys must be depressed while the desired key is being pressed:

CONTROL
SHIFT
REPEAT
[COMMAND]

The following key need only be pressed and then followed by pressing the desired key:

(ESC)



ERASE PAGE

To clear the screen press the ERASE PAGE key. This will return the cursor to its home position and you are ready to start again in the CRT mode. NOTE: in DISK BASIC mode it has erased the screen, but it did not erase your BASIC command internally.

REPEAT

The REPEAT key next to the space bar allows you to type one letter again and again by typing a letter and holding the REPEAT key down at the same time.

CPU RESET

The CPU RESET key, on the far right of the keyboard, when pressed, takes you out of the DISK BASIC mode and puts you into the CRT mode.

The ESCAPE key (ESC), located directly below the AUTO key (top left) permits you to go into various special modes by pressing (ESC) and the desired code key. The keys with a name enclosed within ( ) are standard escape codes. A detailed listing of these codes can be found in Section III.

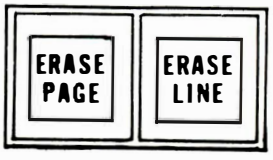
ATTN/BREAK (Attention/Break) KEY

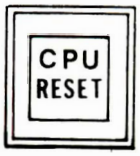
To temporarily suspend operation when running or listing a BASIC program, press the BREAK key.

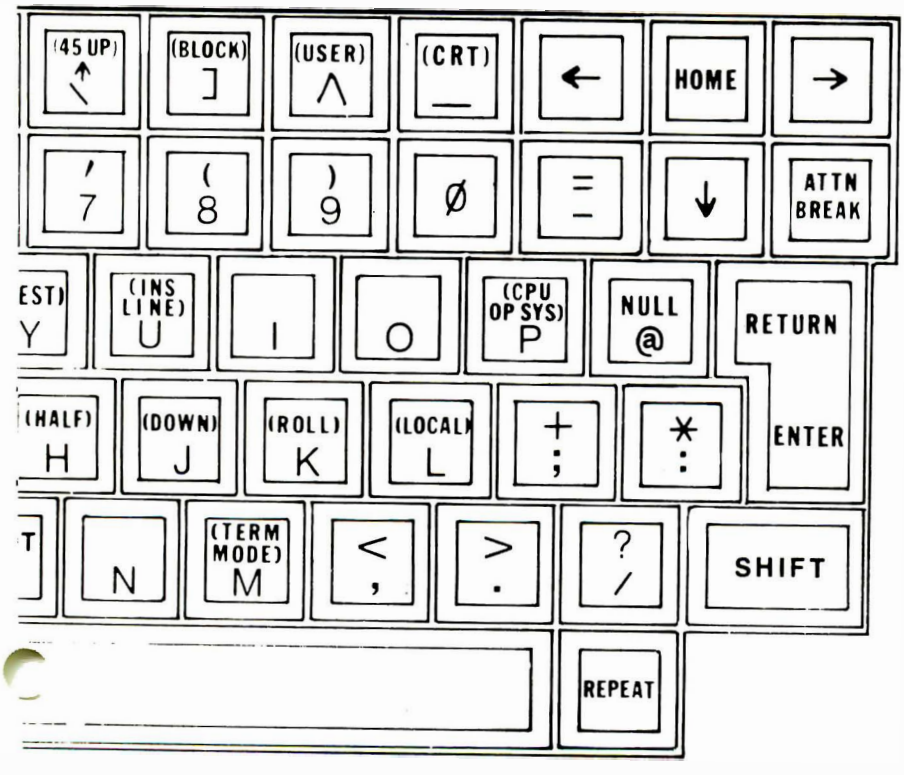
To continue, press RETURN or any other character except ↓.

The ↓ or line feed will cause BASIC to break and halt operation.

Use ↓ followed by RETURN to break out of an INPUT statement in BASIC.







NOTE: There is a difference between the number Ø and the letter O, and between the number 1 and the letter L on all computer keyboards.

What is a Program?

A series of instructions, stored by the computer is called a program.

Programs are written in a simple language called BASIC. The computer already knows this language and with the help of this pamphlet, you will learn some of the BASIC language in order to communicate with Compucolor II.

Let's begin.

You're about to write a simple program.

First: Press CPU RESET key while holding down the SHIFT key and the CONTROL key.

Screen display will look like this:

```
DISK BASIC 8001 V6.78 COPYRIGHT © BY COMPUCOLOR
MAXIMUM RAM AVAILABLE?
7473 (or 15665, or 32049)
READY
```

Now type:

```
10 PRINT "HI! THIS IS THE START OF SOMETHING WONDERFUL!"
```

Recheck your typed statement.

1. If wrong, use← key (backspace) to retype.
2. If correct, press ENTER key.
3. Type RUN and then press the ENTER key.
4. If you get an ERROR message, retype the whole line, beginning with 10.
5. Press the ENTER key.
6. Type RUN and then press the ENTER key.

Did Compucolor follow your instructions?

Congratulations! You have just written your first program!
True, it's only a one-liner, but it is the start of something wonderful!

HIGHLIGHTS

In writing a program every line must have a number. The program is listed on the screen in numerical order, from the smallest to the largest number.

Always use the *numeral Ø* to type your program numbers. The *letter O* cannot be substituted for a number.

Type PRINT: The computer will print everything that is included within the quotation marks.

Press ENTER: This is a command that tells Compucolor II to remember the most recent instruction entered.

Type RUN: Any time you want Compucolor II to follow your instructions, you must type RUN and then press the ENTER key. This causes the Compucolor II to execute the RUN command.

Programs can be expanded.

In the last section you wrote a one-line program. By adding a second or third line, your program can be expanded.

Type
20 PRINT "CAN YOU BELIEVE THAT I CAN WRITE A PROGRAM?"
Check your work for errors.
Press ENTER.
Type RUN and then press the ENTER key.
If all systems worked, the screen display should read:
THIS IS THE START OF SOMETHING WONDERFUL!
CAN YOU BELIEVE THAT I CAN WRITE A PROGRAM?
Let us assume that you want to answer the above question—
Type YES.
Hit ENTER.
Screen display now reads:
SN ERROR.
SN ERROR is the computer's way of telling you that it is not programmed to understand your message. Unless the computer gives you a choice between YES and NO, you cannot enter YES. Sometimes SN ERROR appears even if you do not intentionally enter misinformation.

Type LIST. press ENTER. Behold! The computer has followed your command and has listed everything that you have written.

IF YOUR LISTING HAS A MISTAKE

When you find a mistake, type the number of the line that has the mistake in it. Then retype it correctly and press ENTER. The computer will now incorporate this new line into the program and the original line will be taken out automatically.

SN ERROR

The computer's way of telling you that it cannot understand your message.

LIST

This allows you to see what you have written up to this point.

REMEMBER

Do not press SHIFT key. Letters are printed in capitals. Hold SHIFT key down to get special symbols.

Usually the line numbers in a program are written 10 numbers apart. This numbering system permits you to add new information to your program. Sometimes it is easier to read a program output when there is a space between the lines. To put a space between your program lines—

Type 15 PRINT
Press ENTER
Type RUN

When you type PRINT and write nothing after it, the computer will do just that—it will print a blank line. Pretty neat!

By adding additional numbers and statements, you can expand your program further. Just type in the number and the computer will automatically put it in the correct numerical sequence.

Now that you have taken part in the excitement of programming, you might want to find out more about it. Section 5 of this handbook lists some books on programming and games that might interest you.

HIGHLIGHTS

1) Order
2) RUN
3) SN ERROR
4) LIST
5) SHIFT key

Section III
Summary of Commands

1. CRT COMMANDS

CONTROL CODES

CODE	EXPLANATION
0—NULL (control @)	Has no effect.
1—AUTO (control A)	Loads and runs a BASIC program named "MENU," from the disk drive.
2—PLOT (control B)	Enters graphic plot mode (see plot submodes), not allowed as a BASIC input character.
3—CURSOR XY (control C)	Enters X-Y cursor address mode for either visible cursor or blind cursor, used to go from BASIC to CRT MODE when typed as a BASIC input character.
4—(control D)	Not used.
5—(control E)	Not used.
6—CCI (control F)	The next character which follows provides the 8 bit visible status word. Specifies Foreground, Background, Blink, and Plot. (See status word format, page 9.)
7—BELL (control G)	Not used.
8—HOME (control H)	Moves the cursor to top left corner of display.
9—TAB (control I)	Causes cursor to advance to next column—the tab columns are every 8 characters.
10—↓ (control J) or LINEFEED	Causes a break in BASIC execution of a program, causes the cursor to move down one line.
11—ERASE LINE (control K)	Causes the cursor to return to beginning of line and causes the complete line to be erased. Also causes the BASIC input line to be ignored.
12—ERASE PAGE (control L)	Causes the complete screen to be erased and the cursor moves to the home position. BASIC input ignores this character.
13—RETURN (control M)	Causes the cursor to move to the beginning of the line it presently is on. Causes BASIC input to accept the typed line and process as a statement or input data.
14—A7 ON (control N)	Turns the A7 flag on. (2x character height and also 1 stop bit.)
15—BLINK/A7 OFF (control O)	Turns the blink bit and A7 flag off.
16—BLACK KEY (control P)	Sets foreground color black if flag is off and background black if flag is on.
17—RED KEY (control Q)	Same as above with color red.
18—GREEN KEY (control R)	Same as above with color green.
19—YELLOW KEY (control S)	Same as above with color yellow.
20—BLUE KEY (control T)	Same as above with color blue.
21—MAGENTA KEY (control U)	Same as above with color magenta.
22—CYAN KEY (control V)	Same as above with color cyan.
23—WHITE KEY (control W)	Same as above with color white.
24—XMIT (control X)	Causes data to be transmitted from the visible cursor to the end of the page or until FF, ØØ sequence is found in refresh RAM. Sends text characters with a linefeed and carriage return at end of each line. NOTE: color status is not sent.
25—CURSOR RIGHT (control Y)	Causes the cursor to move right 1 position. On BASIC input displays previous character inputted.
26—CURSOR LEFT (control Z)	Causes the cursor to move left 1 position. On BASIC input deletes previous character from input buffer.
27—ESC (control [)	Provides an entry to the escape code table—must be followed by one or more codes for proper operation.
28—CURSOR UP (control \)	Causes the cursor to move up one line.
29—FG ON/FLAG OFF (control])	Sets the flag bit off. If followed by one of the color keys it will set the foreground to that color. In plot mode OR's "ON" bits.
30—BG ON/FLAG ON (control ^)	Sets the flag bit on. If followed by one of the color keys, it will set the background to that color. In plot mode XOR's "ON" bits.
31—BLINK ON (control —)	Sets the blink bit on which will blink the foreground color against the background color.

ESCAPE CODES

5 BIT CODE	LETTER	FUNCTION
0	@	Used for terminal control—not available for any other use.
1	A	Blind cursor mode.
2	B	Plot via color pad.
3	C	Transmit cursor X, Y position to RS232 PORT.
4	D	Enters Disk File Control System (FCS) with CRT as output.
5	E	Re-entry to DISK BASIC.
6	F	Sets full duplex mode, not functional when in BASIC.
7	G	Enters Disk File Control System (FCS) with RS232 PORT as output.
8	H	Sets half duplex mode.
9	I	Causes a program jump to location 36864.
10	J	Sets write vertical mode.
11	K	Sets roll up and write left to right mode.
12	L	Sets local mode.
13	M	Sets all output to the RS232 PORT.
14	N	Sets to ignore all inputs.
15	O	Not used.
16	P	Not used.
17	Q	Not used.
18	R	Baud rate selection mode. A7 on = 1 stop bit, A7 off = 2 stop bits. (See baud rate table.)
19	S	Causes a program jump to location 40960.
20	T	Causes a program jump to location 33280.
21	U	Not used.
22	V	Not used.
23	W	Initializes and transfers control to DISK BASIC 8001.
24	X	Sets terminal to page mode and write left to right mode.
25	Y	Test mode—fill page with next character.
26	Z	Not used.
27	[	Visible cursor mode.
28	\	Not used.
29	]	Not used.
30	^	Causes a program jump to location 33275.
31	_	Transfer control to the CRT mode.

BAUD RATE SELECTION

Number	1	2	3	4	5	6	7
Baud rate	110	150	300	1200	2400	4800	9600

STATUS WORD FORMAT

A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
Plot	Blink	Background Color			Foreground Color		
		Blue	Green	Red	Blue	Green	Red

INCREMENTAL DIRECTION CODES

	△X1		△Y1		△X2		△Y2	
If BIT = 1	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
Direction	+	−	+	−	+	−	+	−
Value (Hex)	80	40	20	10	8	4	2	1

GRAPHIC PLOT SUBMODES

DISK BASIC plot value or RS-232 INPUT CODE	PLOT SUBMODE	OPTIONAL FUNCTION KEYBOARD CODE
255	Plot Mode Escape	F 15
254	Character Plot	F 14
(253)	X Point Plot	F 13
(252)	Y Point Plot	F 12
251	X-Y Incremental Point Plot	F 11
250	X_0 of X Bar Graph	F 10
(249)	Y of X Bar Graph	F 9
(248)	X max of X Bar Graph	F 8
247	Incremental X Bar Graph	F 7
246	Y_0 of Y Bar Graph	F 6
(245)	X of Y Bar Graph	F 5
(244)	Y max of Y Bar Graph	F 4
243	Incremental Y Bar Graph	F 3
(242)	X_0 Vector Plot	F 2
(241)	Y_0 Vector Plot	F 1
240	Incremental Vector Plot	FØ

For incremental plot submodes see the format of the incremental direction codes (page 9).

2. DISK BASIC

BASIC Statements
The following summary of BASIC statements defines the general format for the statement and gives a brief explanation of its use.

COMMAND	EXPLANATION
CLEAR	Sets the array and string buffers to nulls and zeroes.
CLEAR X	Sets space for string variable to X characters (normally 50 characters).
CONT	Continues execution after CTRL/J, or ↓.
DATA value list	Used in conjunction with READ to input data into an executing program.
DEF FN X (argument) = expression	Defines a user function to be used in the program.
DIM variable (n), variable (n,m), variable $(n), variable $(n,m)	Reserves space for lists and tables according to subscripts specified after variable name. Up to 255 dimensions.
END	Terminates program execution.
FILE "N", "filename", records, rec. size, blocking factor	Creates a new random file with the specified number of records (1-32767), record size (1-32767 bytes), and blocking factor (1-255). File name is a string expression containing a valid FCS file name.
FILE "R", file number, "filename", buffers	Opens a random file with the specified file number (1-127) and number of buffers (1-255).
FILE "A", file, current rec., records, rec. size, blocking factor	Finds the specified attributes for the currently open file: current record accessed, number of records, record size, and blocking factor.
FILE "C", file 1, ---, file N	Closes the specified files and releases the buffer space.
FILE "D", file 1, ---, file N	Writes any modified buffers immediately for the specified files.
FILE "T", line number	Causes file errors to trap to the specified line number. No line number turns the error trapping off.
FILE "E", file, error, line number	Lets the user determine the disk error number and location of the file error.
FOR variable = expression 1 TO expression 2 STEP expression 3	Sets up a loop to be executed the specified number of times.
GET file N, record, first byte; numeric variable, string variable [byte count]	Reads from the record in the file N starting at the specified first byte (1-255) into the variables in the list. String variables must have a byte count (1-255).

BASIC Statements (Cont.)

COMMAND	EXPLANATION
GOSUB line number	Used to transfer control to the first line of a subroutine.
GOTO line number	Used to unconditionally transfer control to other than the next sequential line in the program.
IF expression GOTO line number	Used to conditionally transfer control to the specified line of the program.
IF expression THEN statement	Used to execute BASIC statements only when expression is true.
INPUT list	Used to input data from the terminal keyboard, prompts with "?".
INPUT "string"; list	Used to input data with the quoted string as the prompt.
LIST	Prints the user program currently in memory on the CRT display.
LIST line number	Prints the program from the line specified to the end.
LOAD "PRGRM1"	Loads a BASIC Program named "PRGRM1" from disk into memory. Names cannot exceed six characters (letters and/or numbers).
LOAD "name.ARY"	Loads the numeric array specified by name from disk. First two characters are the array's name.
NEXT variable	Placed at the end of a FOR loop to return control to the FOR statement.
ON X GOSUB line number list	Multiple GOSUB statement. Will transfer control to subroutine on stated line. However, the RETURN statement placed at the end of each subroutine will cause the next statement following ON GOSUB to be executed.
ON X GOTO line number list	Multiple GOTO statement, will transfer control to stated line number, depending on value of variable.
OUT I,X	Causes the byte X to be output to port I (the range of I is 0 to 255).
PLOT expression	Sends the one byte result of the expression to the terminal. The result must be between 0 and 255.
PLOT list	Sends the list of data to the CRT. Example: PLOT 2, 242, 0, 0, 255.
POKE I,X	Causes the byte X to be placed in memory location I, the range of I is 0 to 65535.
PRINT list	Used to output data to the terminal.
PRINT expression	Prints results of expression.
PRINT expression, expression;	The ; causes the carriage return and line feed to be suppressed. Use , for normal spacing and ; for compressed spacing.
PRINT "string"	Prints a character string.
?	Equivalent to the word PRINT.
PRINT SPC (X)	Prints the specified number of spaces.
PRINT TAB (X)	Used to space to the specified column.
PUT file N, record, first byte; numeric expr., string expr. [byte count]	Writes the expressions in the list to the record in file N starting at the specified first byte. String expressions must have a byte count.
READ variable list	Used to assign the values listed in a DATA statement to the specified variables.
REM comment	Used to insert explanatory comments into a BASIC program.
RESTORE	Used to reset the data block pointer so the same data can be used again.
RESTORE line number	Used to reset the data block pointer to a specified line number.
RETURN	Used to return program control to the statement following last executed GOSUB statement.
RUN	Executes the program in memory.
RUN line number	Executes the program starting at line number specified.
SAVE "PRGRM1"	Saves the BASIC program or data from memory into the disk and names it "PRGRM1."
SAVE "name. ARY"	Saves the numeric array specified by name on disk. First two characters are the array's name.
WAIT X,I,J	Causes the input port X to be read, exclusive OR'ed with byte J, and then AND'ed with byte I. The program will wait until the result is zero before continuing.
:	A colon is used to separate multiple statements per line. Example 10 A = 1: B = 10: C = 111

BASIC Operators

SYMBOL	FUNCTION
=	Assignment, or equality test (DISK BASIC 8001 does not allow the LET statement)
−	Negation or subtraction
+	Addition or string concatenation
*	Multiplication
/	Division
^	Exponentiation
NOT	Logical or One's complement (2 byte integer)
AND	Logical or Bitwise AND (2 byte integer)
OR	Logical or Bitwise OR (2 byte integer)
=, <, >, <=, =<, >=, =>, <>	Relational tests (result is TRUE = − 1 or FALSE = 0)

The precedence of operators is:

(1) Expressions in parentheses
(2) Exponentiation (A ^ B)
(3) Negation (−X)
(4) *,/
(5) +,−
(6) Relational operators (=, <>, <, >, <=, >=)
(7) NOT
(8) AND
(9) OR

Standard Mathematical Functions
The Mathematical functions are of the following form: 10y = ABS (x).

NAME	EXPLANATION
ABS(x)	Returns the absolute value of X.
ATN(x)	Returns the arctangent of x as an angle in radians in the range + or − pi/2. Where pi = 3.14159.
CALL(x)	Call the user machine language routine at location 33282. D,E registers have value of X and A,B registers must have Y on return from machine language routine.
COS(x)	Returns the cosine of x radians.
EXP(x)	Returns the value of e^x where e = 2.71828.
FNx(y)	Returns the value of the user defined function x with argument y.
FRE(x)	Returns number of free bytes not in use.
INT(x)	Returns the greatest integer less than or equal to x.
INP(x)	Returns a byte from input port x. The range for x is 0 to 255.
LOG(x)	Returns the natural logarithm of x.
PEEK(x)	Returns a byte from memory address x. The range for x is 0 to 65535.
POS(x)	Returns a value 0 to 63 of the print command column.
RND(x)	Returns a random number between 0 and 1.
SGN(x)	Returns a value indicating the sign of x.
SIN(x)	Returns the sine of x radians.
SQR(x)	Returns the square root of x.
TAN(x)	Returns the tangent of x radians.

Standard String Functions
The string functions are of the following form A$ = CHR$(x) or A = ASC(x$)

NAME	EXPLANATION
ASC(x$)	Returns as a decimal number the eight-bit internal code for the first character of string (x$).
CHR$(x)	Generates a one-character string having the ASCII value of x.
FRE(x$)	Returns number of free string bytes.
LEFT$(x$,I)	Returns left most I characters of string (x$).
LEN(x$)	Returns the number of characters in the string (x$).
MID$(x$,I,J)	Returns J characters of string (x$) starting at position I.
RIGHT$(x$,I)	Returns right most I characters of string (x$).
STR$(x)	Returns the string which represents the numeric value of x.
VAL(x$)	Returns the number represented by the string (x$).

BASIC and FILE Error Codes

After an error occurs, BASIC returns to command level and types READY. Variable values and the program text remain intact, but the program cannot be continued and all GOSUB and FOR context is lost.

When an error occurs in a direct statement, no line number is printed.

Format of error messages:

Direct Statement	XX ERROR
Indirect Statement	XX ERROR IN YYYYY

In both of the above examples, "XX" will be the error code. The "YYYYY" will be the line number where the error occured for the indirect statement.

The following are the possible error codes and their meanings:

ERROR CODE	MEANING
BS	Bad Subscript. An attempt was made to reference a matrix element which is outside the dimension of the matrix. This error can occur if the wrong number of dimensions are used in a matrix reference. For instance, A(1,1,1) = Z when A has been dimensioned DIM A(2,2).
DD	Double Dimension. After a matrix was dimensioned, another dimension statement for the same matrix was encountered. This error often occurs if a matrix has been given the default dimension 10 because a statement like A(1) = 3 is encountered and then later in the program a DIM A(100) is found.
CF	Call Function error. The parameter passed to a math or string function was out of range. CF errors can occur due to. a) A negative matrix subscript (A(-1)=0) b) An unreasonably large matrix subscript (>32767). c) LOG-negative or zero argument. d) SQR-negative argument. e) A↑B with A negative and B not an integer. f) A CALL (X) before the address of the machine language subroutine has been patched in. g) Calls to MID$, LEFT$, RIGHT$, INP, OUT, WAIT, PEEK, POKE, TAB, SPC or ON...GOTO/GOSUB with an improper argument.
ID	Illegal Direct. You cannot use an INPUT or DEF statement as a direct command.
NF	NEXT without FOR. The variable in a NEXT statement corresponds to no previously executed FOR statement.
OD	Out of Data. A READ statement was executed but all of the DATA statements in the program have already been read. The program tried to read too much data or insufficient data was included in the program.
OM	Out of Memory. Program too large, too many variables, too many FOR loops, too many GOSUB's, too complicated an expression or any combination of the above.
OV	Overflow. The result of a calculation was too large to be represented in BASIC's number format. If an underflow occurs, zero is given as the result and execution continues without any error message being printed.
SN	Syntax error. Missing parenthesis in an expression, illegal character in a line, incorrect punctuation, etc.
RG	RETURN without GOSUB. A RETURN statement was encountered without a previous GOSUB statement being executed.
US	Undefined Statement. An attempt was made to GOTO, GOSUB or THEN to a statement which does not exist.
/0	Division by Zero.
CN	Continue error. Attempt to continue a program when none exists, an error occurred, or after a new line was typed into the program.
LS	Long String. Attempt was made by use of the concatenation operator to create a string more than 255 characters long.
OS	Out of String Space. Use the CLEAR X statement to allocate more string space or use smaller strings or fewer string variables.
ST	String Temporaries. A string expression was too complex. Break it into two or more shorter ones.
SL	SAVE/LOAD error. (From disk operation.) Other error messages may also appear from the FILE CONTROL SYSTEM (FCS).
TM	Type Mismatch. The left hand side of an assignment statement was a numeric variable and the right hand side was a string, or vice versa; or, a function which expected a string argument was given a numeric one or vice versa.
UF	Undefined Function. Reference was made to a user defined function which had never been defined.

BASIC and FILE Error Codes (Cont.)

ERROR CODE	ERROR NUMBER	MEANING
EV		No error vector.
BF	2	Bad file name.
NO	4	File not open.
AO	6	File already open.
FS	8	File size error.
RO	10	Record overflow.
EF	12	End of file.
CO	14	Can't open file (usually nonexistent file).
CC	16	Can't close file (usually hardware problem).
RE	18	FCS READ error (usually hardware problem).
WE	20	FCS WRITE error (usually hardware problem).

3. FCS (File Control System) COMMANDS

File Control System is entered by pressing (ESC), then D from the keyboard, or PLOT 27,4 from BASIC. (Only the first three letters of the command need to be typed in.) If (ESC), D is from the keyboard then BASIC is terminated and must be re-entered by (ESC),E key sequence.

Statement Definitions

The following definitions will be used to describe the FCS commands:

( ) Means mandatory part.

[ ] Means optional part and if not specified, will result in the default type.

(Device name:) = [Device type] [Number] (:)

Device types are CD, MD, and FD for Compucolor Disk, Mini-Disk, and 8" Floppy Disk and number is either Ø or 1.

(Memory spec) = (Load address) (Byte count) or (-End address) all memory addresses are in HEX format.

(File spec) = (File name) [.Type] [;Version]

File name is any 6 characters. Type can be any three characters and PRG is default type. Version is Ø to FF HEX number.

NOTE: After a default device type has been selected only the number of the device is required. COMPUCOLOR II defaults to CDØ.

COMMANDS	
COPY [Device Name:] (File Spec) TO [Device Name:] (File Spec)	Will copy one file from one location to another location.
DELETE [Device Name:] (File Spec)	All file spec options are required. Allows the user to delete any file.
DEVICE [Device Name:]	Sets and displays the current default device name.
DIRECTORY [Device Name:]	Lists directory of the default or specified device.
DUPLICATE (Device Name:) TO (Device Name:)	Will duplicate all the files on the original diskette onto another diskette. (Requires two disk drives.)
EXIT "FCS"	(ESC) and (ESC) again or (ESC) and E to return to BASIC.
INITIALIZE [Device Name:] (Volume Name) No. OF DIR BLOCKS	Number of directory blocks will default to a normally adequate no.; NOTE: device name requires all options.
LOAD [Device Name:] (File Spec), Load Address	Loads memory with a program. Defaults to LDA type files written by Compucolor II assembler.
READ [Device Name:] (Start Block No.) (Memory Spec)	Will read into memory from anywhere on the diskette starting at any block and ending where specified, without regard to program boundaries.
RENAME [Device Name:] (File Spec) TO (File Spec)	Allows the user to rename any file to any other name.
RUN [Device Name:] (File Spec)	Loads and executes program by name; normally a PRG type file.
SAVE [Device Name:] (File Spec) (Memory Spec), Start Address, Actual Address	Start address defaults to LOAD address and actual address defaults to load address. Saves memory as a PRG type default file.
WRITE [Device Name:] (Start Block No.) (Memory Spec)	Same as READ but writes memory to diskette. WARNING: it is possible to destroy the FCS directory and file information on a diskette with this command.

FCS Error Codes

EBLF BAD LOAD FILE SPEC, 2
EBLK INVALID BLOCK NUMBER, 2
ECOP ERROR DURING COPY, 1 & 3
ECFB CAN'T FIND BLOCK, 3
EDCS DATA CRC ERROR, 3
EDEL DELETE ERROR, 1 & 3
EDFN DUPLICATE FILE NAME, 2
EDIR DIRECTORY ERROR, 1 & 2
EDRF DIRECTORY FULL, 4
EDSY DATA SYNC CHAR ERROR, 1 & 3
EDUP ERROR DURING DUPLICATE, 1 & 3
EFNF FILE NOT FOUND, 2
EFRD FILE READ ERROR, 3
EFWR FILE WRITE ERROR, 3
EHCS HEADER CRC ERROR, 3
EIVC INVALID COMMAND, 2
EIVF INVALID FUNCTION, 2
EIVD INVALID DEVICE, 2
EIVP INVALID PARAMETERS, 2
EIVU INVALID UNIT, 2
EKBA KEYBOARD ABORT, 4
EMDV MISSING DEVICE NAME, 2
EMEM MEMORY ERROR DURING READ, 4
EMFN MISSING FILE NAME, 2
EMVN MISSING VOLUME NAME, 2
EMVR MISSING VERSION, 2
ENSA NO START ADDRESS, 2
ENVE NO VOLUME ENTRY IN DIRECTORY, 5
ERSZ FILE TOO LARGE TO READ INTO ALLOCATED MEMORY, 2 & 4
ESIZ DEVICE SIZES NOT SAME, 1
ESKF SEEK FAILURE, 1
ESYN SYNTAX ERROR, 2
EVFY VERIFY FAILURE DURING WRITE, 3
EVOV VERSION NUMBER OVERFLOW, 4
EWRF WRITE FAILURE, 3
EWSF FILE TOO LARGE TO WRITE ON DISKETTE, 2 & 4

Descriptions of Solutions to FCS Errors

1.) Mechanical Problem—Jammed READ/WRITE head, loose disk drive internal I/O connectors. Refer to Compucolor Maintenance Manual.

2.) Invalid User Input—Incorrect entry from user. Refer to FCS Commands, page 14.

3.) Diskette Failure—Try a different diskette.

4.) Error Message is self-explanatory.

5.) Diskette Not Initialized—You need to initialize the diskette and possibly purchase a formatted Compucolor blank diskette.

Section IV
Software

Available Software

Compucolor II has an ever growing library of software designed to challenge, stimulate, educate, and facilitate. Check your dealer for the latest available program diskettes.

Precautions/storage

Each 5¼" diskette comes in a folder. For extended media life of your diskette, we suggest the following procedures.

1.) Do not put fingers on the precision surface.
2.) Insert the diskette carefully into the disk drive.
3.) Keep the diskette far from magnetic fields which will erase the diskette.
4.) Store the diskette in the jacket when not in use.
5.) Handle the diskette with care. Bending and folding will damage it.
6.) Diskettes are best stored at temperatures ranging from 10° to 52° C or 50° to 125° F.
7.) Do not leave diskette in disk drive while turning your Compucolor II on or off.

Availability of Preformatted Diskettes—Diskettes are available at the rate of 2 diskettes for $19.95 and may be obtained from Compucolor Corporation or your local dealer.

Precautions/Power Outages

Your Compucolor II should not be operated during an electrical storm. Storms can cause power outages to your Compucolor II. If your machine has a power failure, all data and programs will be lost. If the disk drive is being used during power failure, the diskette may be damaged.

Do not leave diskette in disk drive while turning your Compucolor II on or off.

Section V
Bibliography

Some introductory books on computers and programming available through your Compucolor dealer:

COMPUCOLOR BASIC Manual

AN INTRODUCTION TO MICROCOMPUTERS,
Adam Osborne
Volume 0: The Beginner's Book
Volume 1: Basic Concepts

Basic BASIC,
James S. Coan

A Guided Tour of Computer Programming in BASIC,
Thomas A. Dwyer and Michael S. Kaufman

BASIC (New 2nd Edition),
Bob Albrecht

A Quick Look at BASIC,
Donald D. Spencer

My Computer Likes Me...When I Speak BASIC

What to do After You Hit RETURN

Fun with Computers and BASIC,
Donald D. Spencer

Also check these home-computer oriented magazines, each with its own flavor.

BYTE, Creative Computing, Interface Age, Kilobaud, People's Computers, Personal Computing

Section VI

PORT ASSIGNMENTS

PORT #		I/O PORT ADDRESS
Hex	Dec	
0 — F		TMS 5501
10 — 1F		TMS 5501 Duplicate Addresses
20 — 5F		Not assigned.
60 — 6F		SMC 5027
70 — 7F		SMC 5027 Duplicate Addresses
80 — FF		Not assigned.

PORT #		SMC 5027 CRT CHIP
Hex	Dec	
60 —	96	Load Register 0—Don't Load
61 —	97	Load Register 1—Don't Load
62 —	98	Load Register 2—Don't Load
63 —	99	Load Register 3—Don't Load
64 —	100	Load Register 4—Don't Load
65 —	101	Load Register 5—Don't Load
66 —	102	Load Register 6—Roll Register #
67 —	103	Processor Load Command—Don't Use
68 —	104	Read Cursor X Register
69 —	105	Read Cursor Y Register
6A —	106	Issue Reset Command—Don't Issue
6B —	107	Scroll up 1 line
6C —	108	Load Cursor X Register
6D —	109	Load Cursor Y Register
6E —	110	Load Start Timing—Don't Load
6F —	111	Self Load Command—Don't Use.

PORT #		TMS 5501 I/O CHIP
Hex	Dec	
0 —	0	Read Serial Data in from J-2.
1 —	1	Read Parallel Data from Keyboard Connection J-1.
2 —	2	Read Interrupt Address on TMS 5501.
3 —	3	Read Status on TMS 5501.
4 —	4	Issue Discrete Command.
5 —	5	Set Baud Rate on J-2 Serial I/O.
6 —	6	Transmit Serial Data out to J-2.
7 —	7	Transmit Parallel Data on Connection J-1 (also controls Disk R/W).
8 —	8	Load Interrupt Mask Register.
9 —	9	Interval Timer #1.
A —	10	Interval Timer #2.
B —	11	Interval Timer #3.
C —	12	Interval Timer #4.
D —	13	Interval Timer #5.
E —	14	No Function.
F —	15	No Function.

KEY MEMORY LOCATIONS

28672 to 32767 = Screen refresh RAM.
32978 = Points to maximum RAM used by BASIC.
32982 = Points to end of source and start of variables.
32984 = Points to end of variables and start of arrays.
32986 = Points to end of arrays.
33209 = 0 to 59 seconds of Real Time Clock.
33210 = 0 to 59 minutes of Real Time Clock.
33211 = 0 to 23 hours of Real Time Clock.
33215 = User ESCAPE ↑ jump vector.
33218 = User output FLAG jump vector.
33221 = User input FLAG jump vector.
33224 = User timer no. 2 jump vector.
33238 = External output port buffer.
33247 = Keyboard FLAG.
33249 = FCS output FLAG.
33251 = Input port FLAG.
33265 = BASIC output FLAG.
33272 = Output port FLAG.
33273 = LIST output FLAG.
33278 = Keyboard character.
33279 = Keyboard character ready FLAG.
33282 = Location of CALL(x) jump.
33285 = BASIC output vector location.
33289 = No. of characters on terminal output.
33433 = Start of BASIC source code.
65535 = Maximum amount of RAM.

FIFTY PIN BUS

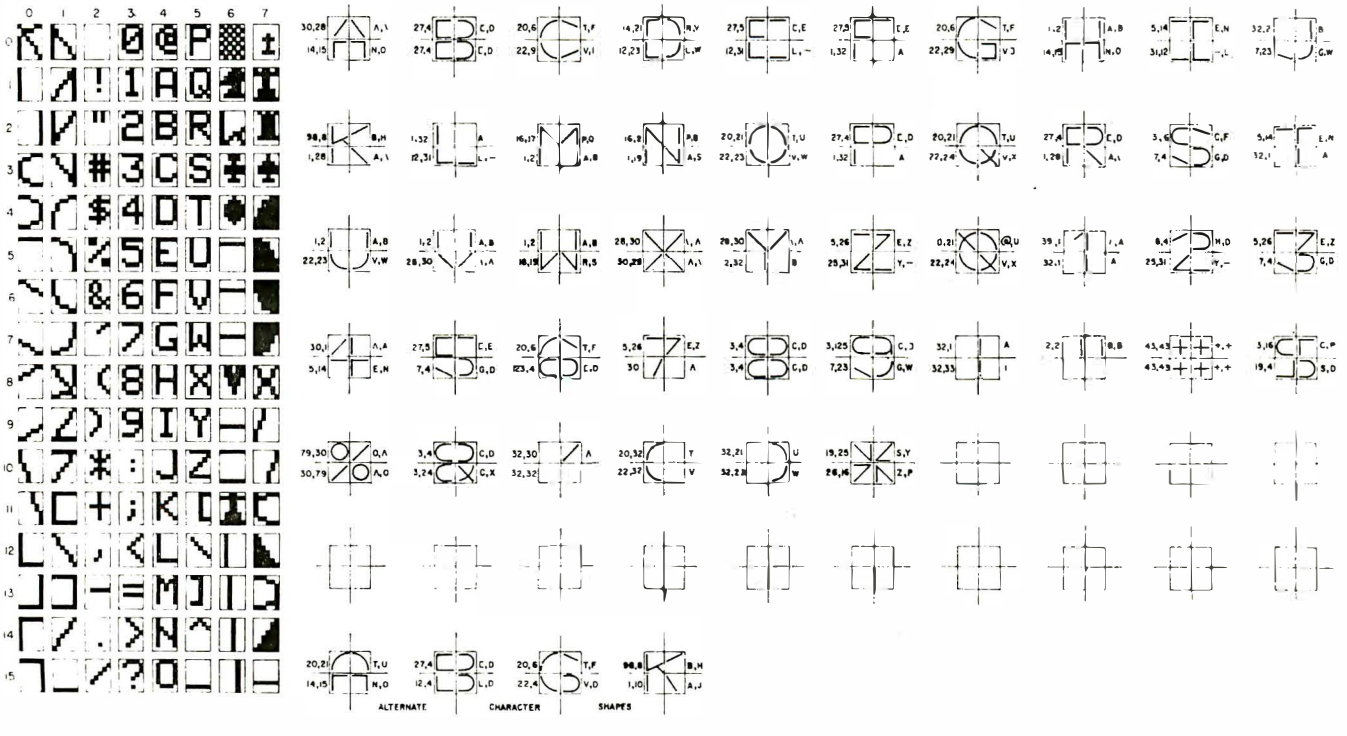
(Preliminary, subject to change.)

PIN	DESIGNATION	PIN	DESIGNATION
1	+12V	26	D2 BUS
2	$\overline{MR}$	27	A2
3	$\overline{MW}$	28	D3 BUS
4	$\overline{I/OW}$	29	A3
5	Φ2 (+12V)	30	D7 BUS
6	Φ2 TTL	31	A4
7	Φ1 (+12V)	32	D6 BUS
8	17.9712MHz	33	D4 BUS
9	SYNC	34	D5 BUS
10	$\overline{RESET}$	35	A6
11	−5V	36	DØ 8080
12	+5V	37	A7
13	GND	38	D1 8080
14	$\overline{I/OR}$	39	A8
15	A 1Ø	40	D2 8080
16	READY	41	A14
17	NO CONNECTION	42	D3 8080
18	NO CONNECTION	43	D4 8080
19	HOLD	44	A9
20	A5	45	A13
21	A11	46	D7 8080
22	DØ BUS	47	A12
23	AØ	48	A15
24	D1 BUS	49	D5 8080
25	A1	50	D6 8080

RS 232C INTERFACE

CPU EDGE CONNECTOR #	RS232C PIN #	SIGNAL NAME AND LINE
1	1	AA Protective Ground
3	2	BA Transmitted Data
5	3	BB Received Data
7	4	CA Request to Send
14	7	AB Signal Ground
15	20	CD Data Terminal Ready

CHARACTER SET



SECTION IV
COMPUCOLOR II SYSTEM DESCRIPTION

IV. SYSTEM DESCRIPTION

A. SOFTWARE

Compucolor II is organized with a software orientation, with excellent versatility a result. All basic functions are under control of the microcomputer.

The microcomputer is constructed around a general purpose microprocessor that handles 8-bit words, has a repertoire of 78 instructions, and can address up to 64K of memory. It connects to a memory access data input/output bus, to which the Keyboard, the Disk Drive, the CRT Display and the telecommunications interface modem also are connected.

The microcomputer memory consists of random access read-only and read/write semiconductor integrated circuits. The read-only segment of memory contains the system operating programs. One part of the read/write segment is used to store video display information that is repeatedly read out of the memory to refresh the CRT display screen. The remainder of the read/write segment is used to store microcomputer programs and other data as an application requires.

MODEL	REFRESH RAM	RAM	ROM	ADDRESS TOTAL
1	8K *	4K	16K	28K
2	8K	8K	16K	32K
3	8K	8K	16K	32K
4	8K	16K	16K	40K
5	8K	32K	16K	56K

*NOTE: Refresh RAM is 4K physically. However, it uses two 4K blocks of addresses - - one 4K block for high speed access for certain operations (such as page erase) and the other 4K block for lower priority functions.

Plug-in connectors are provided for increasing both RAM and ROM. Add-on RAM or ROM may be used so long as the total address capability of 64K is not exceeded. Address assignments are shown on the Memory Map. (See Drawings Section.)

A variety of consumer oriented programs are available on pre-formatted 5¼" diskettes from Compucolor dealers.

B. HARDWARE

The Compucolor II unit includes seven major subassemblies, with major functions as follows:

CRT & CABINET	8-color visual display and unit housing.
POWER ASSEMBLY	Conversion of 115VAC to unregulated DC, low-voltage AC and 60 Hz. sync.
ANALOG ASSEMBLY	Regulated voltages for system; CRT sweep and convergence currents; bias, focus and anode voltages.
LOGIC ASSEMBLY	Data programs and processing for control of video display; sync signals to Analog.
VIDEO ASSEMBLY	Amplification of video signals from logic; CRT connections and bias adjustment.
DISK DRIVE	Data storage and retrieval.
KEYBOARD	Manual data input and control.

The Block Diagram outlines the data and signal flow in the Compucolor II. Interconnecting cabling is shown in the Wiring Diagram. Descriptions of the subassemblies follow in the next section. The Block and Wiring Diagrams are in the Drawings Section.

SECTION V
COMPUCOLOR II SUBASSEMBLY DESCRIPTION

V. SUBASSEMBLY DESCRIPTIONS

A. CRT, YOKE and CABINET

The Compucolor II 8-color display unit is a 13 inch cathode ray tube 13VAXP22. It is secured in the cabinet by a spring harness and has a yoke assembly containing the deflection and convergence coils. The CRT and yoke are similar to standard TV components.

Connections to the CRT are through a socket on the Video Board and two HV leads. Connections to the yoke assembly are through connectorized cables from the Analog Board.

The required voltages and signals for the CRT have sources as follows:

Filament voltage -	6.3 VAC from the Power Board via the Video Board.
Screen control -	200 VAC from the Analog Board and adjusted by three potentiometers on the Video Board.
Cathode return -	Through a common resistor on the Video Board to ground.
Video input -	Signals from the Logic Board through driver amplifiers on the Video Board to CRT control grids.
Focus voltage -	Approximately 4KV by separate lead between CRT socket on Video Board to HV Supply attached to Analog Board. Fine adjustment potentiometer mounted on Analog Board frame.
Anode -	20KV by separate lead from HV Supply on Analog Board to CRT HV connector.

Deflection and convergence currents for the yoke assembly are developed in the Analog Board from timing pulses supplied by the Logic Board.

B. POWER BOARD

The Power Board is mounted in the rear cover of the cabinet. Its circuit is shown in the upper right portion of Analog Schematic Drawing 100902 (or 100903). It supplies unregulated 150 VDC and 15 VDC, 6.3 VAC and Vertical Sync. The 3 - wire power cord for 115 VAC input connects to this unit. Line fuse F1 (2.5 A.,slow blow) is located on the Power Unit. The ON-OFF switch SW 1 is mounted on the Power Board and is operated from outside the back of the cabinet. There is a line filter. Varistors protect against voltage spikes.

+ 150 VDC is supplied by bridge rectifier BR2, with filtering by capacitor C2. The +150 VDC source has additional fusing in F2 (1.5 A., fast acting) located in the Power Unit.

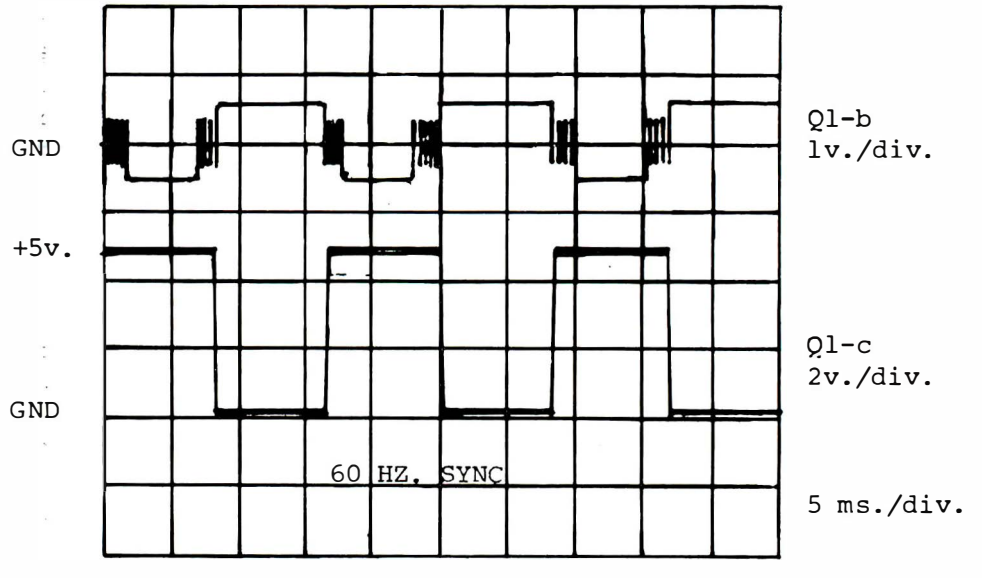
CAUTION: Note that the +150-volt supply is not referenced to frame ground. It has a "hot" common. Special precautions are required for measurements.

The +150 VDC is used directly in the horizontal sweep circuit and the switched regulator on the Analog Board and indirectly, via the switched regulator, in almost all other parts of the system.

+15 VDC is supplied by bridge rectifier BR3, with filtering by capacitor C7. AC input to the rectifier is from the full secondary of stepdown transformer T1. The +15 VDC supply is referenced to frame ground. +15 VDC is used directly in the horizontal sweep circuit and the switched regulator on the Analog Board. Failure of the +15 VDC supply will result in loss of the regulated voltages required by most parts of the system.

6.3 VAC for the CRT filament is supplied by one-half the secondary winding of stepdown transformer T1. It is connected to the CRT through the Video Board.

Vertical Sync Generator Q1 is located on the Power Board. Low voltage 60 Hz. from transformer T1 is applied to the base of Q1 through current limiting resistor R2. The negative-going portion of the waveform is clipped by diode CR1 and the positive-going portion by the transistor base-emitter junction. The collector load resistor and supply voltage are located in the Analog Board. The collector output rectangular waveform goes to the Logic Board by way of the Analog Board.



Waveforms at F2 and C7+, though not shown, are essentially DC with noise and ripple normally 6.0 and 1.0 volts peak-to-peak respectively.

C. ANALOG BOARD

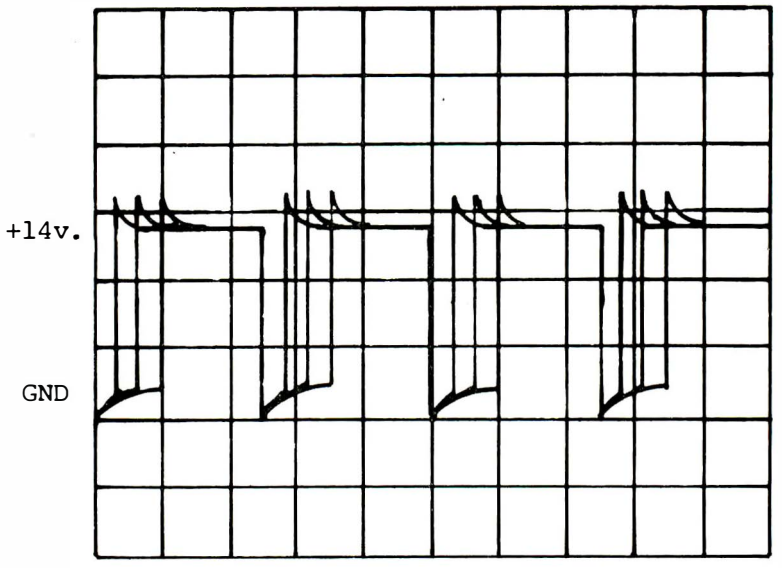
The Analog Board is mounted in the side portion of the Compucolor II cabinet, beside the CRT. It provides regulated low voltages used throughout the system, horizontal and vertical sweep currents and convergence signals for the CRT yoke assembly, and 200 VDC for the CRT screen controls. A high voltage unit attached to the Analog Board supplies the CRT focus and anode potentials. The Focus potentiometer is mounted in the frame of the Analog Board. Schematic Drawing 100902 shows the circuits involved.

Regulated low voltages are developed by a switching regulator from unregulated 150 VDC and 15 VDC furnished by the Power Board. The right hand side of the Analog Schematic shows the circuit.

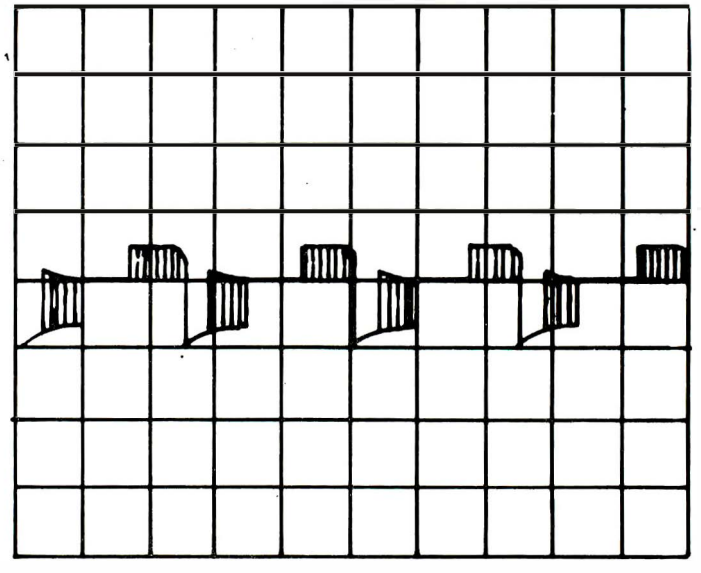
U3 and associated components generate a square wave at approximately 20 KHz. to drive power amplifier transistors Q6 and Q7. These transistors provide the input to transformer T4. The T4 secondary delivers the 20 KHz. square wave at several voltage levels to bridge rectifiers BR1 and BR2 and to full-wave rectifier CR3 and CR4. Regulation is achieved by control of the supply voltage to Q6 and Q7. U2, Q5 and associated components perform this function.

U2 generates a variable-width pulsed waveform (approximately 20KHz.) to control the duty cycle of Q5. The pulsed waveform applied to the Q5 base-emitter junction causes Q5 to conduct for the positive-going pulse duration. Since Q5 is in series with the voltage supply to Q6 and Q7, widening of the positive-going pulse causes Q5 to conduct a greater portion of the time and increase the nominally 100VDC supply to Q6 and Q7. When the positive-going pulse is made more narrow, the supply to Q6 and Q7 is decreased. Feedback from the +5V Regulated output at BR1 causes U2 and Q5 to adjust the supply to Q6 and Q7 as required to keep the +5V Regulated level constant.

U2 and U3 are SG3524 integrated circuits requiring input DC in the range of 8 to 40 volts across pins 15 (+) and 8 (-). In this instance both U2 and U3 have pin 8 at frame ground and pin 15 to +15VDC from the Power Board. One output, at pin 16, is a well regulated nominally +5VDC; it is used as a reference in control of the switched regulator but also is available for other usage in currents up to 50 mA. The frequency of the U2 pulsed output is controlled by R24 and C4. The positive-going pulse time is determined internally by comparison of a portion of the feedback voltage (at pin 1) to a portion of the reference voltage (pin 2). R22 provides feedback adjustment and is used to set the +5V Regulated output at the correct level. The output variable-pulse-width waveform is available across collector-emitter combinations CA-EA (pins 12 & 11) and CB-EB (pins 13 & 14). In the case of U2, the connection to the primary of transformer T2 is from only the CA-EA combination.



The U2 - generated pulses applied to Q5 through T2 results in Q5 being turned on for varying portions of the waveform period. The Q5 output is a chopped DC waveform, which is filtered by L1 - C34.



U3 also generates a rectangular waveform, with output connections at terminals 11 through 14, but its circuit differs from that of U2 in two respects:

1) Both output combinations CA-EA and CB-EB are used to drive transformer T3.

2) The feedback is fixed to yield a symmetrical square wave at the output.

R44, R45 and R43 provide the references to obtain the square wave. R47-C28 set the frequency to approximately 20 KHz.

NOTES CONCERNING REVISED ANALOG BOARD

The Analog Board description contained in pages 5.03 through 5.15 covers the board used in the first several hundred production units. A redesigned board, introduced in 1979, has fewer parts and an improved component layout. The newer schematic is Rev.4; the newer PCB layout is Rev.3.

The basic functions of the board remain unchanged. The locations of the major circuit subdivisions on the schematic drawing are the same. However, there are a number of changes in components and component reference designations. This sheet outlines the major changes, many of which involve the convergence circuits.

1. A single DG300 IC (U5 on revised schematic) replaces Q12, Q13, Q14, Q15 and several associated components. The reset pulses, horizontal and vertical, now cause their respective sections of DG300 to operate for discharge of the ramp capacitors. (C83 is the horizontal ramp capacitor, C84 the vertical.)

2. Two sections of a TL084 IC (U6) replace two 741's for charging the ramp capacitors. Two other sections in the TL084 serve as comparators to generate square waves from the sawtooth ramps.

3. A DG303 (U7) replaces the 4016 bilateral switch. It requires only two comparators for switch operation instead of the four required by the 4016.

4. Only +8 and -8 regulated voltages are needed by these IC's. VR1 supplies the -8V. as before. VR2 supplies +8V. and replaces a voltage divider.

5. Generation of the parabola and pincushion waveforms is unchanged.

Other Changes:

6. In the horizontal voltage regulation circuit, the MC741 (U1) is supplied by its own rectifier rather than by a voltage divider (originally R48-R10). CR24, connected to a primary tap of T4, provides +20V. referenced to the 150-volt common.

7. In the horizontal pincushion circuits Q10 has been eliminated. All of the correction is applied to the horizontal voltage regulator via the optical coupler.

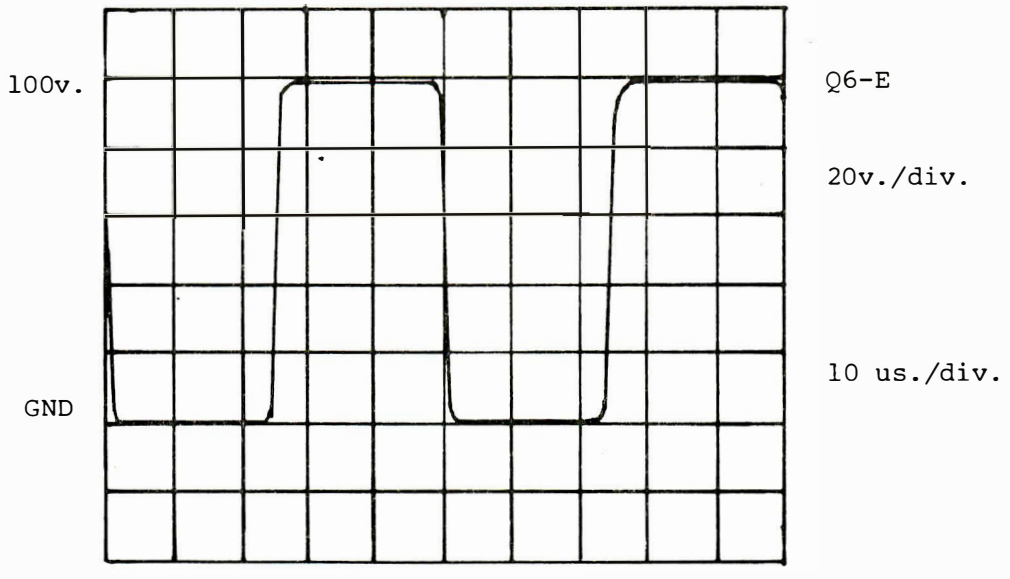
8. Q11, once considered for power supply sync, is no longer shown near the right-hand SG3524.

9. The NE540 IC's in the convergence and vertical sweep amplifier circuits are supplied with +12 volts rather than +11 volts. (Q17, Q18 and Q19 still use +11V.)

10. Vertical pincushion correction is fixed, eliminating one potentiometer.

11. Voltage limiting diodes have been added at the +5V. and +12V. rectifier outputs for circuit protection.

The 20 KHz. square wave is applied to the primary of T3 to drive push-pull amplifier transistors Q6 - Q7. The amplitude that these transistors deliver to the primary of transformer T4 is dependent upon the momentary level of the supply voltage at Q6-C. This voltage, as described earlier, is regulated by U2-Q5 to be the level required to keep the +5V Regulated output constant.



The regulated low-voltage DC outputs are obtained from rectifiers BR1, BR2 and CR3-CR4, each with output filtering. Although feedback from only the +5V Regulated is used for voltage control, the loads on the other outputs are sufficiently stable to consider these other voltages also regulated. All of these voltages are referenced to frame ground. They supply circuits as follows:

-48 V. Video Board driver amplifiers.
Analog Board horizontal and vertical ramp reset circuits.

±12V. Logic Board circuits
Analog Board horizontal and vertical ramp, parabola and pincushion circuits.

±11-volt outputs through resistors R50 and R51, with additional filtering for the convergence and vertical sweep amplifiers.

-8-volt reference through VR1 for ramp generators.
+8-volt level through voltage divider R91-R98 for the convergence signal switches in U5.

±5V. Logic Board circuits.
CRT cathode bias

In addition to the voltages listed above, there are two other reference voltages, with lower current capabilities, used in the Analog Board:

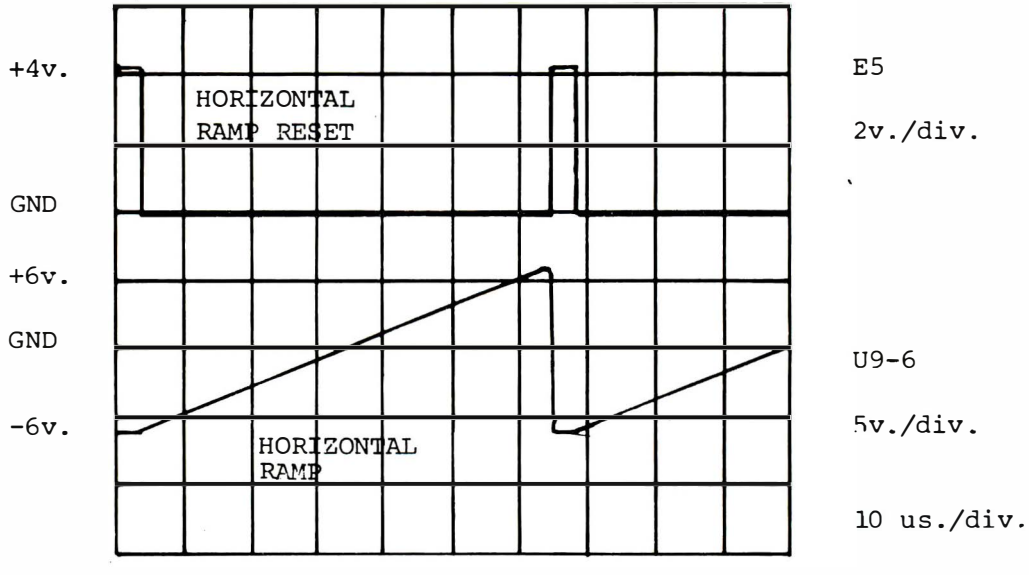
+5V. REF1 — From U2-pin16. Referenced to frame ground. Used in the horizontal sweep generator, the vertical sync generator (collector supply for Q1 on Power Board) and the horizontal pincushion optical coupler.

+3.9V.REF2 — From CR3. Referenced to 150V "hot" common. Used in horizontal sweep generator circuits.

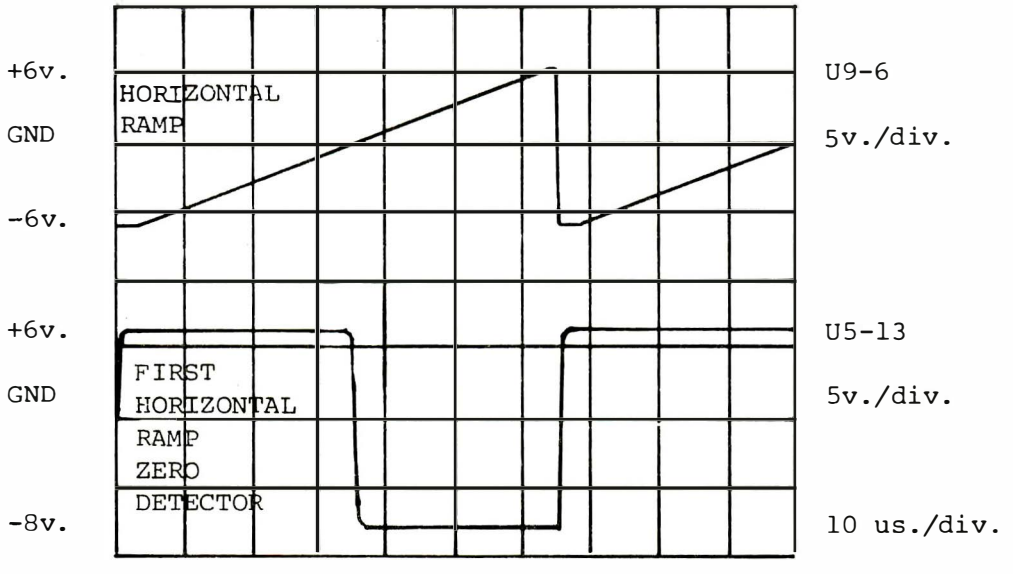
None of the regulated low voltages and reference voltages should have noise or ripple exceeding 3 % other than the ±11V. supply for the vertical sweep amplifier.

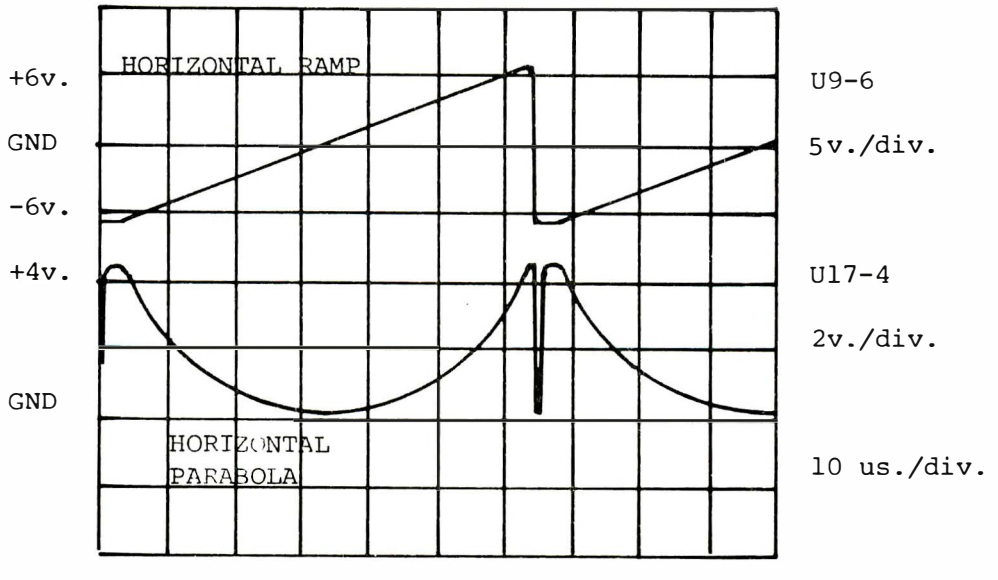
Convergence Circuits are shown in the upper left portion of Analog Schematic 100902. These include horizontal ramp and parabola, vertical ramp and parabola, pincushion, switches to develop signals for each of four quadrants, and a convergence amplifier.

The horizontal ramp sawtooth is generated across capacitor C48 by operational amplifier U9. The rate of voltage rise across C48 is adjusted by R102 to equalize the ramp positive and negative points at U9-6. The steep discharge portion of the sawtooth occurs when FET Q13 conducts. Normally the E111 is biased off by the -48V. through R59 and CR17. However, when the Horizontal Ramp Reset pulse from the Logic Board causes Q12 to conduct, the resulting positive-going pulse at the Q12 collector is coupled by capacitor C47 to the gate of Q13 to turn on the FET for discharge of C48. As soon as the reset pulse has passed, the -48V. again biases Q13 off and the linear charge of C48 begins anew. The waveform at U9-pin6 is a linear sawtooth with a period of approximately 65 us.

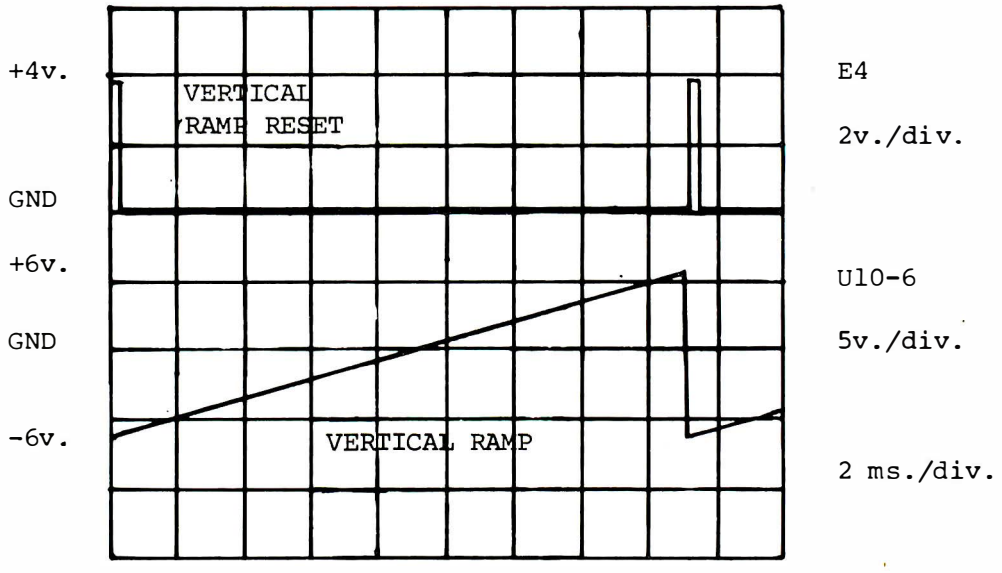


This horizontal ramp is passed through comparators in U8 to apply square waves to pins 5 and 13 of the bilateral switches in U5. Pin 13 is positive during the first half of the ramp, pin 5 during the second half. The horizontal ramp also is connected to the input of analog multiplier U17 to develop the horizontal parabola applied to other inputs of U5 at pins 2 and 3. (The output at pin 4 of U17 is one-tenth of the product of the two inputs at pins 1 and 6. Since the horizontal ramp - call it "X" - is applied to both inputs, the output - call it "Y" - then is $Y=X^2/10$, the formula of a parabola.) R102 is adjusted to equalize the amplitude of the right and left parabola end points. R101 is used to adjust the DC offset of the parabola to bring the parabola center to ground.



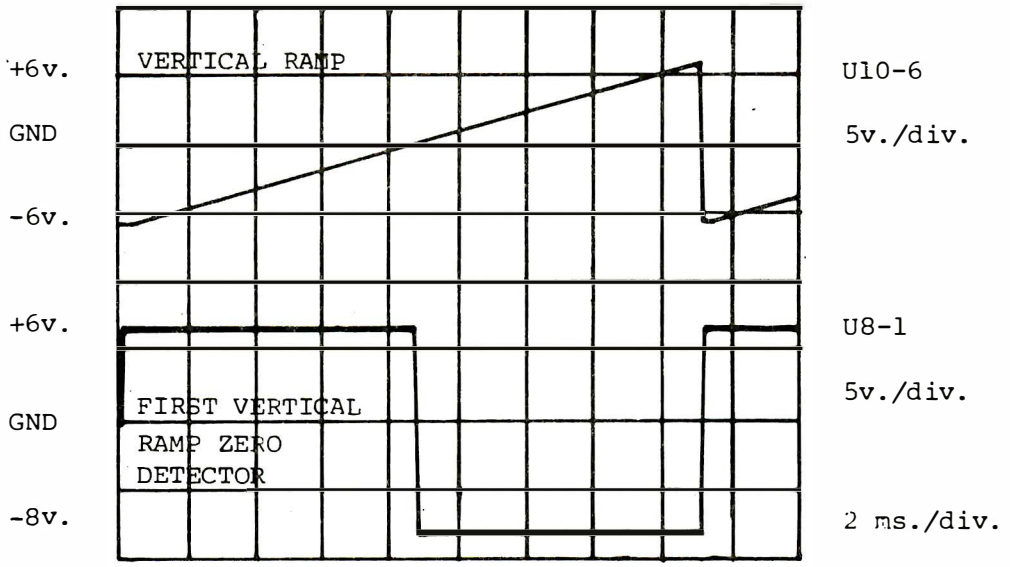


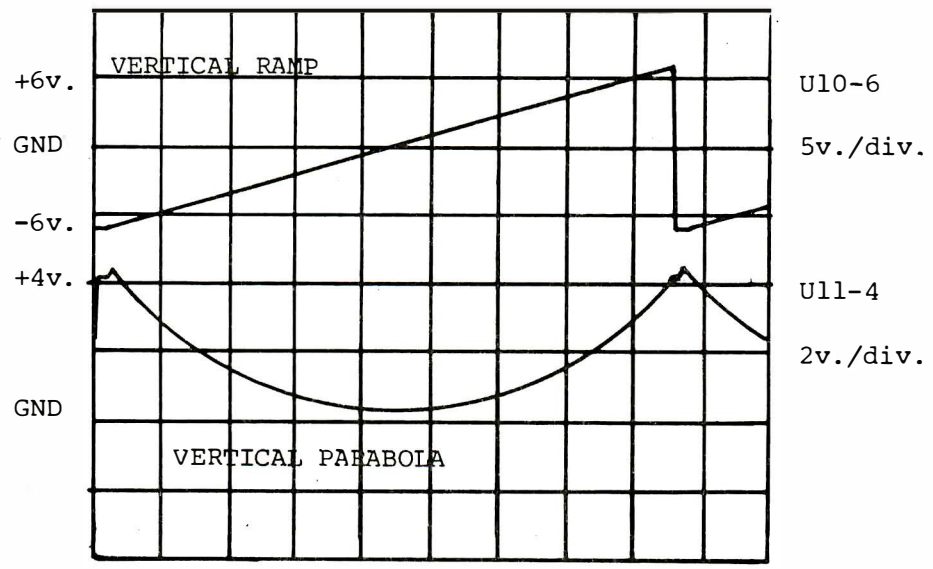
The vertical ramp and parabola are generated in similar fashion. Operational amplifier U10 requires more time to charge the larger sweep capacitor C50. The charging rate is adjusted by R103. The wider Vertical Ramp Reset pulse through Q14 to FET Q15 results in longer turn-on of Q15 and a slight dead time between C50 discharge and initiation of the next ramp. However, this dead time is a very small percentage of the total ramp time and is less noticable in the vertical than in the horizontal ramp.



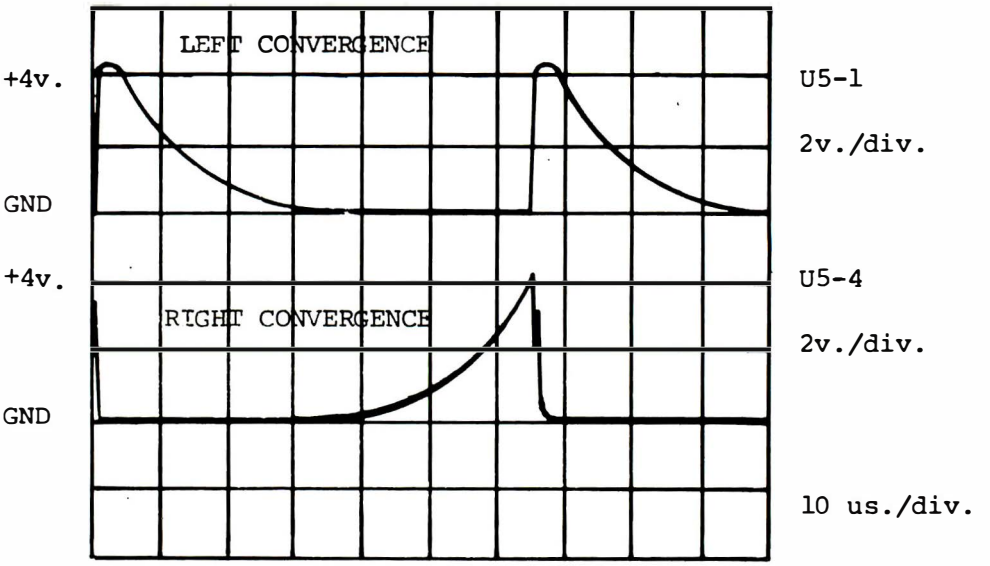
The vertical ramp is also passed through comparators in U8 to switches in U5, with pin 6 of U5 receiving a positive signal during the first half of the ramp and pin 12 a positive signal during the second half. The vertical parabola is applied to other inputs at pins 9 and 10.

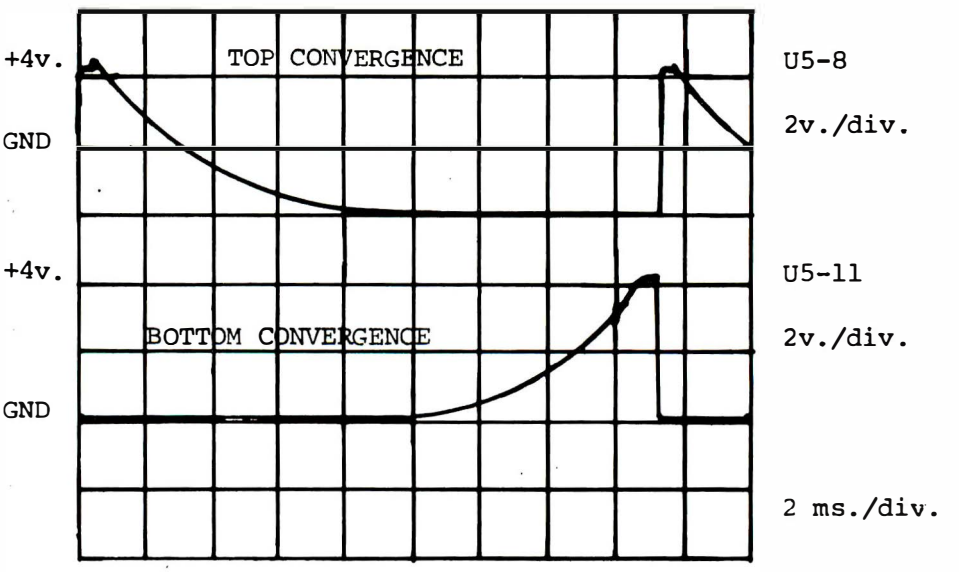
The vertical parabola is developed in U11. Adjustment of R103 equalizes the heights of the parabola end points. Adjustment of R104 brings the parabola center to ground level.


+6v.
GND
-6v.
+6v.
GND
-8v.
VERTICAL RAMP
FIRST VERTICAL
RAMP ZERO
DETECTOR
U10-6
5v./div.
U8-1
5v./div.
2 ms./div.


+6v.
GND
-6v.
+4v.
GND
VERTICAL RAMP
VERTICAL PARABOLA
U10-6
5v./div.
U11-4
2v./div.

Power supply for all four U5 switches is +8V. from R98-R91 to U5 pin 14, and -8V. from VR1 to U5 pin 7. The combination of square wave and parabola waveforms at the switches result in the convergence waveforms.

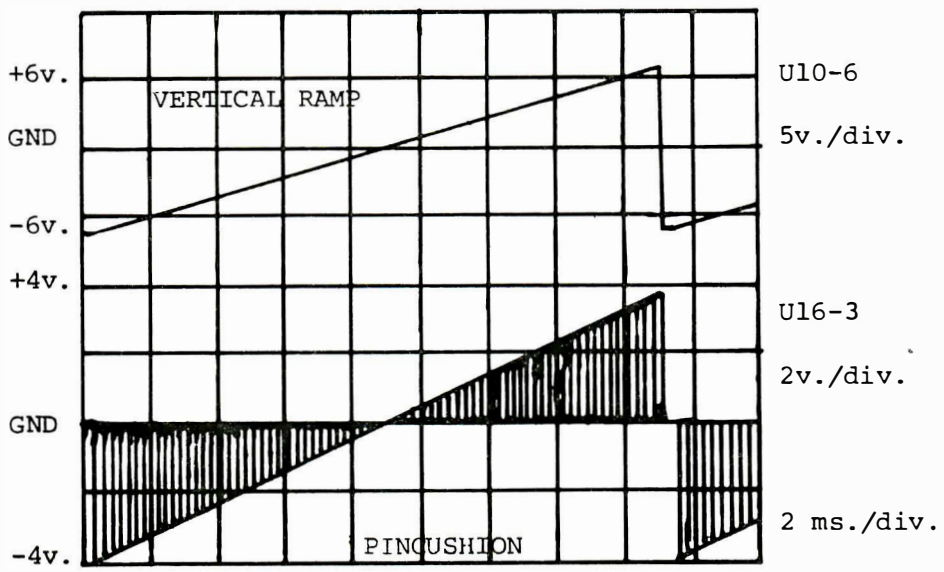




These waveforms from U5 are summed in proportions determined by the adjustments of convergence RIGHT, LEFT, TOP and BOTTOM control potentiometers R95, R94, R96 and R97 and applied to the input of power driver U13.

U13 provides amplification to drive the power amplifier transistor Q17, which has the convergence coil in the CRT yoke assembly as a load. Power supply for both U13 and Q17 is 11 volts. Feedback is provided by R75-C66 and by R76.

The vertical ramp and the horizontal parabola are combined in analog multiplier U16 to produce the pincushion waveform used in the vertical sweep generator.



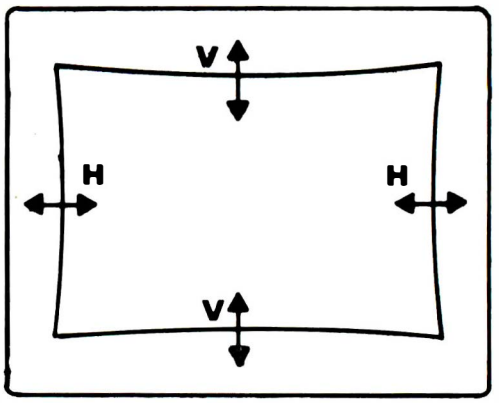
(Horizontal Parabola multiplied by Vertical Ramp)

Vertical Sweep is developed in the circuit shown in the center left portion of Analog Schematic 100902. Power driver U12 receives two signal inputs. The vertical ramp sawtooth input amplitude is adjusted by VERT HEIGHT potentiometer R106 and the pincushion input by VERT PINCUSHION potentiometer R107. The vertical ramp is the basis for vertical sweep. However, it is modified by the pincushion signal to yield equal deflection across the top and bottom of the CRT display.

In the CRT the electron beam travels farther to reach the top corners of the display than it travels to reach the top center. Therefore, for a given amount of angular deflection vertically, the beam strikes the CRT face higher at the top corners than at the top center.

V = Vertical
Pincushion

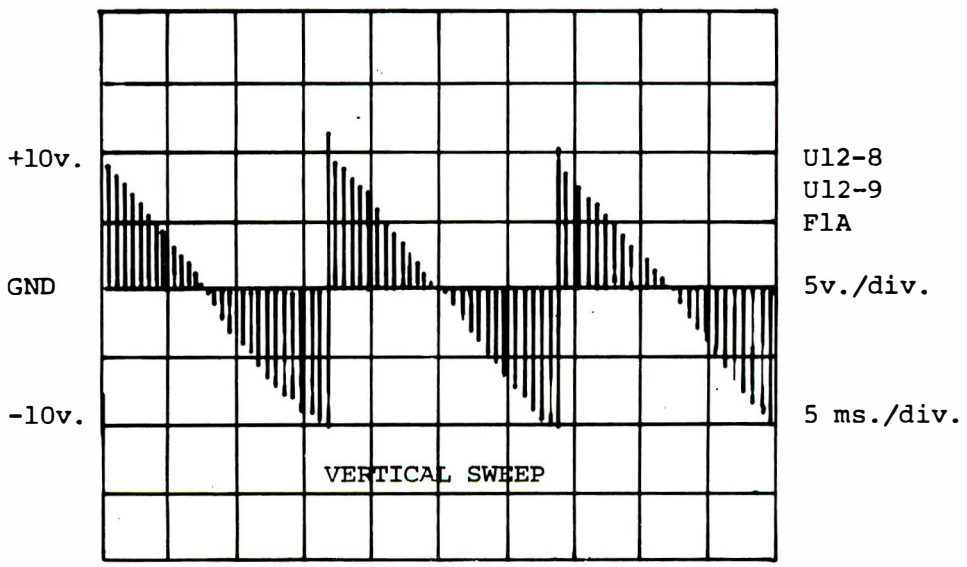
H = Horizontal
Pincushion



Vertical pincushion compensates by slightly reducing vertical angular deflection progressively as the position of the beam horizontally departs from center. The CRT display then has uniform vertical deflection across the top and bottom.

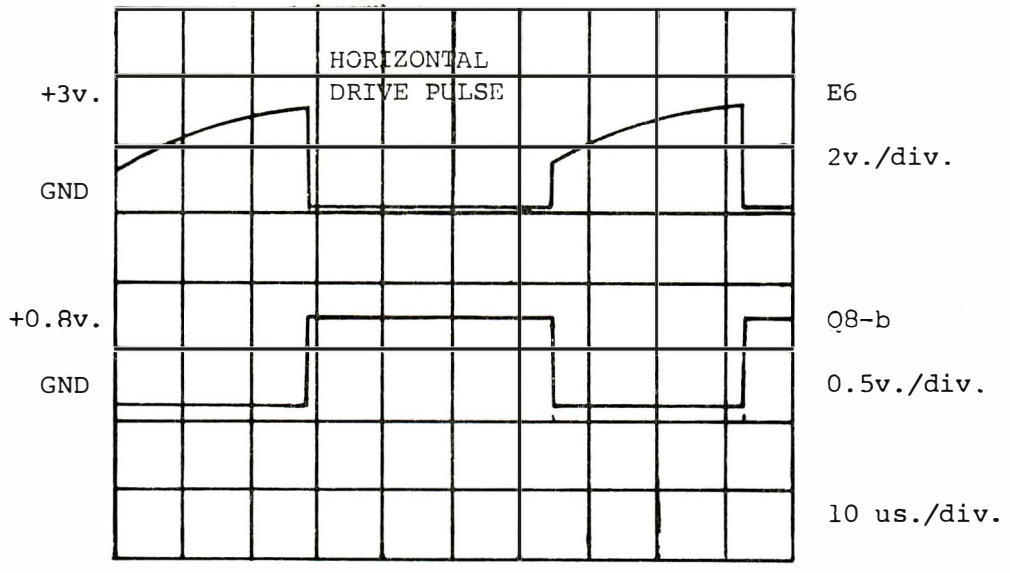
The U12 combines the two inputs and produces two composite outputs to drive power amplifier transistors Q18 and Q19.

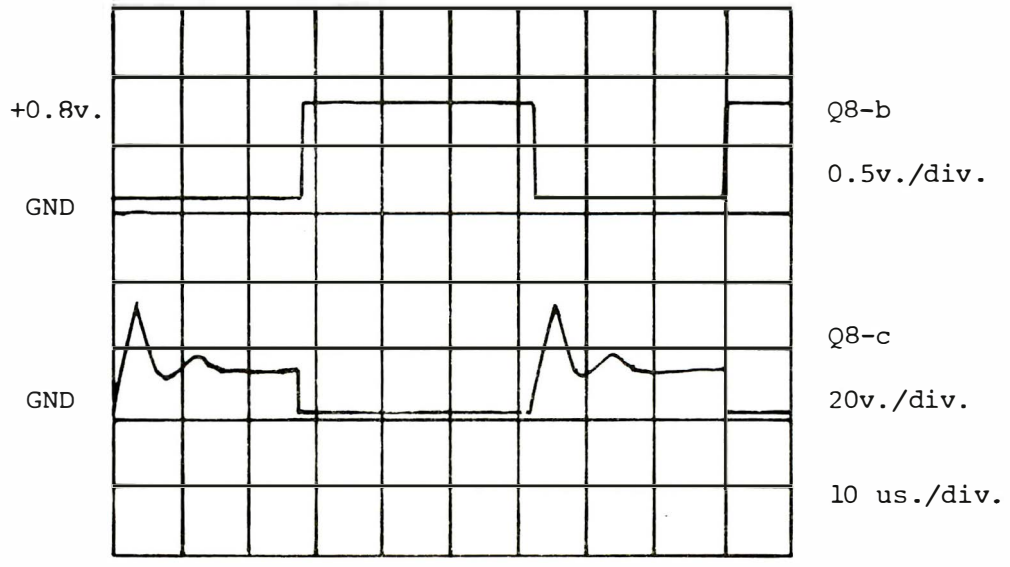
Vertical centering of the sweep waveform is accomplished by adjustment of VERT CENTERING potentiometer R105. Frequency compensated negative feedback to insure linear amplification is applied to pin 4 of U12 from both the power amplifier (network R73-C62-C67-R72) and the vertical deflection coil (via R71). The power amplifier transistors Q18-Q19 have the vertical deflection coil as load. Series protection against shorts is provided by fuse F1A (1.5 A.).



Horizontal Sweep circuits are shown in lower left portion of Analog Schematic 100902.

Sweep timing is furnished by the Horizontal Drive Pulse from the Logic Board to E6. This signal, amplified by transistors Q9 and Q8 and coupled through transformer T1, drives power transistor Q1. The amount of drive is modified somewhat by transistor Q10, which is controlled by the vertical parabola. Q10 thus causes the Q8 collector supply voltage (at T1-7) to be greater when the vertical sweep is at mid-point and lower when the vertical sweep is at top or bottom of the display. (This represents a part of the horizontal pincushion correction.) Q1 pulses fly-back transformer FBT1 through C71. (Note: In earlier models Q10 is omitted.)





Supply voltage for Q9 is +5V REF1 and for Q8 and Q10 it's the +15V unregulated. Both are referenced to frame ground.

The voltage and current to FBT1 is regulated by the circuitry including Q2, Q3, Q4, U1 and U4.

> CAUTION: Note that this is referenced to the 150V. "hot" common, not frame ground.

The unregulated 150V, connected through decoupling filter R17-C17, is regulated by power transistor Q2 to power FBT1. The remainder of the regulator circuit operates to control the conduction of Q2.

Two factors are involved in this control of Q2. One is negative feedback from (a) the Q2 emitter output through R9 to one input of U1 and from (b) the collector of Q4 through C13-C11-R15, also to U1 pin 3. Feedback from both sources is adjusted by HOR WIDTH potentiometer R109. The other factor is the vertical parabola signal through optical coupler U4, with adjustment by HOR PINCUSHION potentiometer R108. The signal from R108 is applied through R12 to the other input of U1. (This is the remainder of the horizontal pincushion correction, omitted from earlier models.)

The LED portion of the optical coupler has +5V REF1, referenced to frame ground, as its supply voltage. However, the photo transistor portion of U4 uses 3.9V REF 2, referenced to the 150V "hot" common. The supply voltages for U1 also are referenced to the 150V common.

The output of U1 is amplified by transistors Q4 and Q3 to control the conduction of Q2. Direct coupling is used. The collector supply for Q4 and Q3 is the unregulated 150V., reduced to approximately 140V. by R17, again with reference to the "hot" common, not frame ground.

FBT1, with current through Q2 and pulsed by Q1, generates the horizontal sweep current for the deflection coil in the CRT yoke assembly.

High Voltage DC, at two levels, is obtained by rectifying parts of the horizontal sweep waveform. From a separate winding of FBT1, the high voltage fly-back pulse is rectified to obtain approximately +20KV for the CRT anode. The rectifier and a voltage divider are in a sealed unit attached to the Analog Board near FBT1. One high voltage lead from this sealed unit has a connector for the CRT anode. Another high voltage lead from this sealed unit is terminated so as to mate with the Focus lead from the Video Board. The focus voltage is obtained from a voltage divider in the high voltage unit. The fine Focus adjustment is mounted on the Analog Board frame and is accessible through a hole in the cabinet rear cover.

Another portion of the horizontal wave form from terminal 1 of FBT1 is coupled through capacitor C30 to a rectifier and filter. The resulting DC voltage, approximately +200V referenced to frame ground, is used for CRT screen control in the Video Board.

Connections to the Analog Board from the yoke are through pins, mounted on the board, and connectorized twisted lead cable. Connections from the

Analog Board to other units are by twisted lead cables originating in the Analog Board and terminated in connectors for easy mating with connectors in other units. There are two ground clips.

E1-E6	To Logic Board (Sweep and convergence sync pulses)
E7-E10	To Power Board (Unregulated DC, 60 Hz. Sync)
E15-E18	To Video Board (DC voltages)
E19-E25	To Logic Board (Regulated DC voltages)
J1	To Yoke Assembly (Vertical Sweep and Convergence)
J2	To Yoke Assembly (Horizontal Sweep)

D. LOGIC BOARD

The Logic Board is mounted in the lower part of the cabinet. It receives input data and, together with the software, processes it for CRT display or for serial transmission to the Disk Controller or to the outside world. Schematic Drawing 100961 shows the circuit which, for discussion purposes, may be treated as a microcomputer and a display generator.

The microcomputer, occupying the left two thirds of the drawing, includes the 8080 Central Processing Unit (UA2), a Clock Generator (UB1) a multi-function Input/Output Unit (UD2) Read Only Memory (UA4-UA7), CRT Refresh Random Access Memory (UD4-UD11), user Random Access Memory (UB4-UB11), and several other devices for selection and control of data processing functions. A Data Bus and an Address Bus provide much of the interconnection.

The display generator, shown on the right one-third of the schematic drawing, includes the 5027 CRT Controller (UF9), Character Generator (UF6-UF7), Character, Status and Color Latches (UE6, UE5, UE4), Shift Register (UF5), Color PROM (UG5), and several additional devices involved in the selection and timing of signals for the CRT display. The CRT Refresh RAM (UD4-UD11) also is part of the display generator.

Data is recieved through either the Serial I/O Ports or the Keyboard. It is processed by the microprocessor and software and routed via the control and data buses to the appropriate circuit. If it is data to be presented on the screen, it is placed in the CRT Refresh RAM along with an appropriate control word to identify the color, blink and graphics status.

Once in Refresh RAM, the data is presented to the display generator circuitry. Here the first of two memory words is processed into an ASCII character or graphics dot pattern; the second word is processed simultaneously into color, blink and graphics identifier information. The resulting serial output of color video information -- red, green, blue -- is coordinated with horizontal and vertical synchronizing signals to synchronize the serial output information with the CRT horizontal and vertical sweep signals generated in the Analog Board.

MICROPROCESSOR

The 8080 CPU and its associated 8224 Clock Generator, 8228 Bus Driver/ Controller and 5501 I/O Controller make up the heart of the Logic Board computer functions.

The 8080 CPU is a general purpose microprocessor that can handle 8-bit words, has a repertoire of 78 instructions and can address up to 64K of memory through the Address Bus. See Appendix for more information.

The 8224 Clock Generator includes a 17.9712 MHz. oscillator, controlled by crystal Y1, and generates timing pulses Ø1 and Ø2 at one-ninth the crystal frequency. (The 17.9712 MHz output from terminal 12 is routed to a number of other units for timing purposes. These will be mentioned as the other units are discussed.)

The 8-line data I/O port of the 8080 CPU connects in parallel to the 8228 Bus Driver/Controller and the 5501 I/O Controller. All data to or from the 8080 CPU passes through one of these two units.

The 5501 I/O Controller passes data to and from the Keyboard and the Disk Controller (and the Data Modem, if used). It handles both serial and parallel data. Data to be sent to the Disk Controller or the Data Modem is converted to serial form and transmitted through the 1488 Line Driver (UG1). Data bits 04 and 05 from the 5501, applied to a NAND gate in UF2 (74LS00), enable transmission to the designated unit. Serial data from the Disk or Modem comes through the 1489 Line Reciever (UD1), also controlled by data bits 04 and 05 from the 5501. See Table below.

UF2				UD1		Built-in	Add-on	Modem
12	13	11	Q2	8	Q1	Disk	Disk	
L	L	H	ON	L	OFF	ON	ON	OFF
L	H	H	ON	L	OFF	ON	OFF	OFF
H	L	H	ON	L	OFF	OFF	ON	OFF
H	H	L	OFF	H	ON	OFF	OFF	ON

Thus when either of bits 04 and 05 is low, the Line Driver and Receiver sections associated with the Disk Controller are enabled. The outputs of the sections associated with the Modem are held high. When both bits are high, the reverse is true. Bit 04 low causes the resident Disk Drive to run. Bit 05 low causes the add-on Disk Drive (connected to a branch of the keyboard cable) to run.

Parallel outputs 0Ø-07 from the 5501, passed through the 81LS95 Octal Buffer (UF1) without inversion, serve both as controls for the Disk Controller and as inputs to the Keyboard. The Keyboard returns 12 lines of information to the Logic Board. Eight of these are multiplexed by the 74LS157 Quadruple 2-line-to-1-line Multiplexer (UE1) onto four lines. These, with four of the original 12, make up an 8-line parallel input to the 5501. The Keyboard also has a RESET input to the Logic Board to reset the microprocessor to its initial condition.

The operation of the 5501 I/O Controller is determined by address bits AØ-A3 from the 8080 CPU. See Appendix for details of the TMS 5501 Multifunction Input/Output device.

The 8228 Bus Driver/Controller handles all other parallel data transfers between the 8080 CPU and a variety of units, including the user Random Access Memory, Read Only Memory, add-on RAM and ROM, CRT Controller and CRT Refresh Random Access Memory. The 8228 reads the status off the 8080 I/O Port data to determine the action to be taken.

As a bus driver, the 8228 provides isolation between the 8080 Data Bus and the memories. As a controller, it issues the Memory Read/Write and Input/Output Read/Write Commands.

The Main Driven Data Bus originates at the 8228 Bus Driver/Controller terminals DBØ-DB7. From there (Schematic Drawing 100961, upper left corner) its eight lines, designated DØ-D7, connect in parallel to the following units:

Description	Function
1) 50-pin bus J3 for add-on units	I/O Data
2) Connector J8 for add-on RAM	I/O Data
3) 8K (or 16K) RAM (UB4-UB11)	I/O Data
4) 81LS95 Octal Buffer (UE7)	Refresh RAM Output Data
5) 4K Refresh RAM (UD4-UD11)	Input Data to Refresh RAM
6) 82S123 I/O PROM (UA1)	CRT Controller Data
7) 16K ROM (UA4-UA7)	ROM Output Data
8) Connector J9 for add-on ROM	Output Data
9) 5027 CRT Controller (UF9)	Input Data to CRT controller (and I/O for Cursor Data)

The CRT Refresh RAM output data, in addition to being connected to the main data bus through Octal Buffer UE7, is connected to the 74LS377 Character Latch UE6 and Status Latch UE5.

The Address Bus is the route over which the 8080 CPU addresses the various memories. This 16-bit parallel data bus originates at the AØ-A15 terminals of the 8080 CPU (near upper left of Schematic Drawing 100961) and extends in whole or in part to the following:

Description	Bits Used
1) 50-pin Bus J3 for add-on units	AØ-A15
2) 3242 Address Multiplexer/Refresh Counter (UA3) (where 14 bits are multiplexed on 7 lines for addressing user RAM and add-on RAM)	AØ-A13
3) 82S129 Address Decoder/Timer for RAM(UE2)	A13-A15
4) 82S123 I/O PROM (UA1)	AØ-A4
5) 82S129 System Decoder (UF3)	A13-A15
6) 5501 I/O Controller (UD2)	AØ-A3

7) 82S123 ROM/PROM Decoder (UB3)	A11-A14
8) 8K ROM (UA4-UA7)	AØ-A12
9) A NAND gate in 74LS00 (UF2)	A7 only
10) Connector J9 for add-on ROM	AØ-A11
11) 74LS153 Multiplexers (UD12, UE9,UE8) (multiplexed with CRT controller outputs to form 6-line addresses to CRT Refresh RAM)	AØ-A11
12) 5027 CRT Controller (UF9)	A8-A11
13) 82S129 CPU & Horizontal Decoder (UF8)	A12 only

Some address inputs to the 82S123 and 82S129 PROM come from other sources.

The Logic Board uses several types of Programmed Read-Only Memories. Four PROMs are used for control purposes in the microcomputer portion.

The 82S129 System Decoder (UF3) is a 256X4 PROM. The 4-bit word output from its memory enables certain Logic Board function:

- DØ is the Chip Enable for the 5501 I/O Controller UD2.
- D1 is the DBIN signal to the 8228 Bus Driver/Controller UB2 to indicate whether the 8080 Data Bus is in an input mode (DBIN high) or an output mode (DBIN low).
- D2 is part of the address to ROM/PROM Decoder UB3, directing use of the Read-Only Memory.
- D3 is the Chip Select signal to the 5027 CRT Controller and part of the address to the CPU & Horizontal Decoder UF8.

The required 8-bit address to the System Decoder comes from several sources:

- AØ is the 8080 CPU DBIN signal.
- A1 is the $\overline{\text{I/O R}}$ signal from the 8228 Bus Driver/Controller.
- A2 and A3 are the D6 and D4 bits (advance I/O R and I/O W) from the 8228, passed through inverters in UC1.
- A4,A5 and A6 are address bits A13-A15 from the 8080.
- A7 is the $\overline{\text{MR}}$ signal from the 8228.

The 82S129 Address Decoder & Timer (UE2) is a 256x4 tri-state output PROM which provides the decoding and timing functions for RAM. Part of its 8-bit address comes from the Address Bus (bits A13-A15). Two bits are the $\overline{\text{Memory Read}}$ and $\overline{\text{Memory Write}}$ commands from the 8228 Bus Driver/Controller. One bit is the Ø2 Clock (TTL level). One is the 8080's $\overline{\text{WR}}$ signal. The remaining bit is the Refresh Signal from the second flip-flop in 74LS74 (UG2, terminals 8-13). The 4-bit words from memory are involved in RAM functions:

DØ is passed through two Schmitt triggers in UD3 to yield the Column Address Strobe to the resident user RAM UB4-UB11.

D1 supplies the Refresh Enable and Count inputs to Address Multiplexer UA3.

D2 through a Schmitt trigger in UD3 supplies the Row Address Strobe to the user RAM UB4-UB11 and to any add-on RAM. Through another Schmitt trigger it supplies the Row Enable signal to Address Multiplexer UA3.

D3 is passed through two Schmitt triggers to yield the Column Address Strobe to add-on RAM.

Thus when the address issued by the 8080 CPU indicates access to RAM -- for either Read or Write -- the Address Decoder and Timer PROM enables the Address Multiplexer UA3 and initiates the generation of strobes to the selected Random Access Memory.

The 3242 Address Multiplexer/Refresh Counter (UA3) receives 14 address bits from the 8080 CPU. It multiplexes these into seven outputs (OØ-O6). These outputs make up the row/column address inputs for the user RAM (UB4-UB11) and/or the add-on RAM.

The Zero Detect output (terminal 15) is an input to one of the two monostable multivibrators in 74LS123 (UG4), which times the Refresh Signal. When the 64 (or 128) cycles of refresh have been completed, Zero Detect goes low to trigger the one-shot multivibrator. When it times out in a bit under 1 ms., a high is generated at terminal 12. This high is applied to the terminal 12 D input of a flip-flop in UG2 and is passed on to terminal 9 on the next low-high transition of the 8224 Clock Generator Ø2 (TTL) signal. This causes the Address Decoder & Timer UE2 to initiate another refresh cycle with high at D1 and at D2.

The Count and Refresh Enable inputs for the 3242 come from the 82S129 Address Decoder and Time (UE2), which also provides the Row Enable signal to the 3242. When terminal 3 of the 3242 is made high, the multiplexer outputs are row addresses; when it is low, the outputs are column addresses.

The User Random Access Memory is made up of eight one-bit-wide Dynamic RAM (UB4-UB11). (4K RAM uses 4115, 8K RAM uses 4116 type chips.) Each supplies one bit of the 8-bit word to be written into or read from memory. The memory cells within are arranged in a matrix of rows and columns. The 14 address bits required to identify a particular cell in the array have been multiplexed on 7 address lines and come into the RAM chips as 7 row address bits followed by 7 column address bits. RAS (Row Address Strobe) and CAS (Column Address Strobe) serve to latch the address into the chip. If data on the Data Bus (connected to chip inputs) is to be written into memory, a negative transition on Write (MW) causes this to occur. If MW is maintained high, data is retrieved from memory and put on the data bus.

The Dynamic RAM memory cells require refresh within 2 ms. intervals. Refresh occurs during each memory cycle. Refresh also occurs every millisecond or less, as described earlier in the paragraphs relating to the 3242 Address Multiplexer/Refresh Counter. A memory output from UE2 causes a Schmitt trigger in UD3 to generate the $\overline{RAS}$ required to refresh the RAM. (Refresh takes place during any cycle in which $\overline{RAS}$ occurs; and when $\overline{RAS}$ is received without $\overline{CAS}$, the memory state is not affected.) Refresh requires 32 us. (64 us. for 128 cycles) for completion.

The 82S123 I/O PROM (UA1) is a 32x8 PROM whose 8-bit words, when read from memory, are delivered on the Data Bus for 5027 CRT Controller start up. The chip is enabled by a combination of the $\overline{I/OR}$ signal from the 8228 Bus Driver/Controller and the A7 bit from the Address Bus. The negative $\overline{I/OR}$ transition causes an inverter in UC1 to apply a high to one input of a NAND gate UF2. If the A7 address bit also is high, the gate output goes low to provide the $\overline{CE}$ for UA1. Address Bus bits AØ-A4 cause the appropriate 8-bit word to be read onto the Data Bus.

The 82S123 ROM/PROM Decoder (UB3) is a 32x8 PROM whose 8-bit output from memory provides a Chip Select to one of the ROM chips UA4-UA7 or one of the add-on ROM at J9.

One of its five address inputs has an option connection to ground or +5V. Normally it is connected to Address Bus bit A11. The optional connections are provided for possible shift from Basic to other software. Three inputs are Address Bus bits A12-14. The fifth input is from the System Decoder UF3.

When ROM is addressed by the 8080 CPU to read data onto the Data Bus, the ROM/PROM Decoder enables the selected ROM chip.

The Read Only Memory (UA4-UA7) normally resident in the Compucolor II has storage capacity for 16K 8-bit words. Options are available to increase this capacity to 24K. A change in the type of ROM chip used will require changes in the option patches associated with power voltages, address inputs and chip select leads. The table following shows the patches.

INPUT →		+12	-5	A12	A10			CS		GND	A11
PATCH NO. →		1	2	3	4	5	6	7	8	9	10
ROM CHIP	2708	X	X					X		X	
	2716	X	X				X		X		
	4732					X		X			X
	9216	X			X			X		X	
	36000			X		X		X			X

When the required address bits are present on the Address Bus, the data from the selected memory area is read onto the Data Bus when the Chip Select signal is received from the ROM/PROM Decoder. Refer to the Memory Map in the Software Description Section for ROM layout.

The CRT Refresh RAM (UD4-UD11) is similar to the user RAM. It has connections directly to the Data Bus for data to be written into memory. Output data from memory can be passed to the Data Bus through 81LS95 Tri-State Octal Buffer UE7 when gated by lows at its terminals 1 and 19. Output data from the CRT Refresh RAM is connected directly to two 74LS377 latches, Character Latch UE6 and Status Latch UE5.

The 6-line address comes from 74LS153 Multiplexers UE8, UE9 and UD12. The address sources include bits AØ-All form the Address Bus, six character counter outputs and five data row counter outputs from the 5027 CRT Controller, and an output of CRT Timing PROM UG8. The Select signals for the Multiplexer originate in the CPU & Horizontal Decoder PROM UF8 and the CRT Refresh RAM Timing Multiplexer UG6. Thus the CRT Refresh RAM is addressed by either the 8080 CPU or the 5027 CRT Controller.

The Refresh RAM, treated as a part of the microcomputer, is also very much associated with the display generator, the description of which follows.

DISPLAY GENERATOR

The 5027 CRT Controller (UF9), under control of the microcomputer, generates CRT frame formatting signals such as horizontal and vertical sync, characters per data row, data rows per frame, row select data, blanking, and cursor video data. (See Appendix for details of the 5027 CRT Controller unit.)

The microcomputer exercises control through a series of 8-bit words on the Data Bus and 4-bit register addresses on the Address Bus. The Chip Select signal is received from the System Decoder UF3. Data Strobe, which strobes DØ-D7 data into the appropriate 5027 register, is the I/OW signal from the 8228 Bus Driver/Controller. The other input to the 5027, Dot Counter Carry, is from the 1.4976 MHz. output of Dot Counter UG7.

Character Counter and Data Row Counter Outputs from the CRT Controller go to the 74LS153 Multiplexers to become part of the address to Refresh RAM. Other outputs of the 5027 are used in generation of synchronizing signals for the Analog Board and in the addressing of PROMs in other parts of the display generator. These are discussed later in this section.

Several PROMs of various types are used in display generation. The uses of these PROMs are taken up next.

The 82S123 CRT Timing UG8 is a 32x8 PROM whose outputs from memory provide timing signals for a number of devices in display generator circuits. One of its five address bits (A4) is the H6 Character Counter output from the 5027 CRT Controller. The other four address bits come from the 74LS163 Synchronous Binary Counter UG7.

The input Clock for that Counter is the 17.9712 MHz. Oscillator signal. With the feedback from the D5 output of the CRT Timing PROM to terminal 1 of the Counter, the output at terminal 11 of the Counter is 17.9712 MHz. divided by 12, or 1.4976 MHz (the character timing frequency, with a period of 667 ns.).

The 8-bit output from the UG8 memory is used as follows:

DØ-D2	Clock inputs to Status, Color and Character Latches UE5, UE4 and UE6. D1 is also the Shift/Load input to Shift Register UF5.
D3&D7	Inputs to CRT Refresh Timing Multiplexer UG6.
D4	Clock input to flip-flop in UG3.
D5	Clear input to Dot Counter UG7.
D6	One address bit to CRT Refresh RAM through Multiplexer UD12.

The 82S129 CPU and Horizontal Decoder UF8 is a 256x4 PROM. Five bits of its 8-bit address are the H2-H6 Character Counter Outputs from the 5027 CRT Controller. One bit is the 5027 Chip Select from the System Decoder. Another bit is theA12 bit from the Address Bus (designating priority of access to the CRT Refresh RAM -- a low gives immediate access). The remaining bit is from a flip-flop in UG3.

The 4-bit output from memory is used for:

DØ	RDYIN signal to Clock Generator UB1 via an AND gate.
D1	Power Supply Sync to the Analog Board.
D2	Timing trigger for the horizontal Drive circuit.
D3	Input signals to a flip-flop in UG3.

The 74LS74 Flip-Flop UG3's terminal 9 output, as the select A control for the CRT Refresh RAM address multiplexers (74S153 terminal 14), determines whether the 5027 or the 8080 address Refresh RAM. As the Select signal to Multiplexer UG6 it causes UG6 to pass the appropriate set of inputs $\overline{MW}$, $\overline{RAS}$,$\overline{CS}$ and $\overline{CAS}$ to Refresh RAM. ("A" inputs when the 5027 is addressing Refresh RAM and "B" inputs when the 8080 is addressing it.) Terminal 9 is low to select 5027 addresses and associated control signals for CRT Refresh RAM. It is high to select 8080 addresses and controls.

The 74LS157 Multiplexer UG6 has two sets of four inputs, one of which is gated to the four outputs by UG3.

INPUT TERM	SET	SIGNAL SOURCE	OUTPUT TERM	SIGNAL USE
2	A	+5V	4	One gate for Buffer UE7
3	B	$\overline{MR}$ from 8228		(low is half of enable)
5	A	D7 from UG8	7	B Select to CRT Refresh
6	B	$\overline{WR}$ from 8080 or $\overline{MR}$ via gates in UF2 & UF4		RAM address multiplexers and $\overline{CAS}$ to Refresh RAM
11	A	+5V	9	$\overline{MW}$ for CRT Refresh RAM
10	B	$\overline{MW}$ from 8228		
14	A	D3 from UG8	12	$\overline{RAS}$ and $\overline{CS}$ for CRT
13	B	$\overline{WR}$ or $\overline{MR}$ via UF2 & UF4		Refresh RAM

The 81LS95 Octal Buffer UE7 passes the CRT Refresh RAM output to the System Data Bus only when the 8080 CPU addresses Refresh RAM.
The components in the upper right portion of Schematic 100961 are associated with the character generation. Each character is defined in a 6x8 matrix, eight scan lines six dots long. Two 8-bit words are required for each character to be displayed. The first word is the "X" address to the Character Generator, which provides the dot pattern. The second word includes foreground color, background color and foreground blink status. These words are stored in the CRT Refresh RAM (32 lines x 64 characters x 2 words each = 4096 words).

The Character Generator UF6-UF7, two 1024 x 8 ROM's, provides storage for words describing 128 characters and a variety of graphics. It holds eight outputs for each character (one for each line of the character). These are accessed by a single "X" address (7 bits) for each character and by eight "Y" addresses (3 bits each).

The 82S129 Scan Decoder UG9 is a 256 x 4 PROM that supplies the "Y" address inputs to the Character Generator with three of its outputs. (The fourth output is Cursor information.) Its address bits include the 5027 CRT Controller's Scan Counter RØ, Row Select R1 & R2, Data Row Counter DRØ and Cursor Video. It also receives the D7 bit of the first character word and a 1.875 Hz. signal from the Blink Counter.

The 74LS393 Blink Counter UG10 input is 60 Hz. sync from the Analog Board through a Schmitt trigger in UE3. It divides this by 32 to yield the 1.875 Hz. blink rate. This is an input to two units in the generation of characters, cursor and graphics and to the 5501 Multifunction I/O Device (SENS, term.22). It is also used for the real time clock.

Three 74LS377 Octal Latches are involved in the processing of the information for characters. Each of these contains eight D-type flip-flops with common Enable and Clock inputs. In this case, with all three Enable inputs at Ground, information at the D inputs is transferred to the Q outputs on the positive-going edge of the Clock pulse. The Clock pulses are generated by the CRT Timing PROM UG8. Output data from the CRT Refresh RAM is applied to the Character Latch UE6 input. The Character Latch output, together with the Scan Decoder UG9 and the R1-R2 outputs of the 5027 CRT Controller address the Character Generator UF6-UF7. An output of the Status Latch enables either UF6 (for characters) or UF7 (for graphics). The parallel 6-bit Character Generator output is changed to serial output by the 74LS166 Dot Shift Register and applied as one input to 82S131 Color PROM U7.

The other word for character generation is, immediately following the input to the Character Latch, addressed from CRT Refresh RAM to the Status Latch UE5. One output of the Status Latch determines which of the two chips of the Character Generator is enabled. Another output bit is applied with the 1.875 Hz. waveform to an AND gate whose output goes to the Color Latch. The other six Status Latch output bits (background and foreground color information) are addressed directly to the Color Latch.

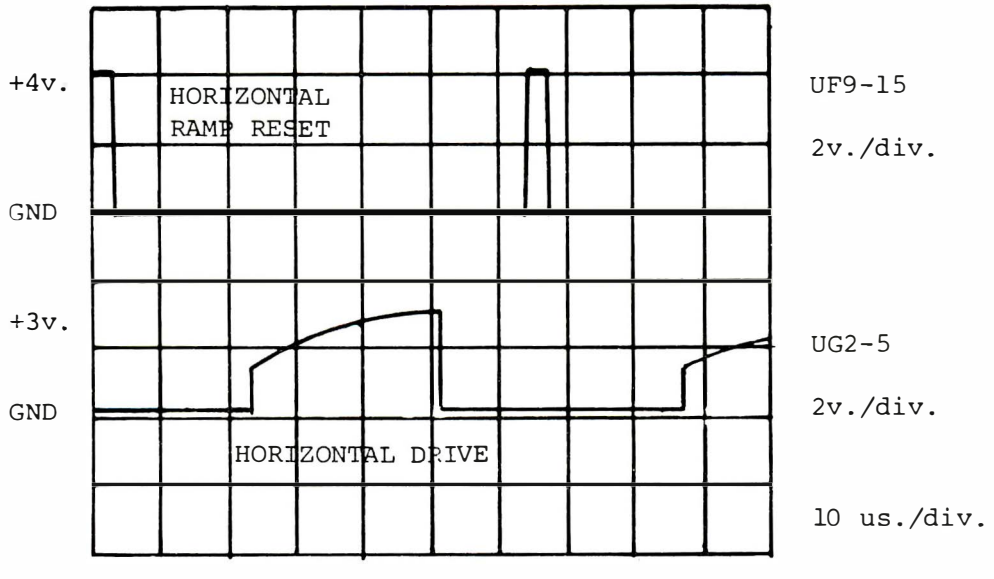
The 74LS377 Color Latch UE4 is set by the seven input bits just described, plus an 8th bit from the Scan Decoder PROM UG9. Its output comprises eight bits of the 9-bit address required by the Color PROM UG5. (The 9th bit is the serial character data from the Dot Shift Register UF5.)

The 82S131 Color PROM UG5 is a 512x4 PROM. Three bits of its possible 4-bit output from memory are the Red, Blue and Green signals to the Video Board. During sweep retrace the Blank pulse from the 5027 disables the Color PROM.

The 5027 CRT Controller generates synchronizing signals for the Analog Board to coordinate the sweep pattern with the video signals from the Color PROM. Two of these are supplied directly:

Horizontal Ramp Reset from H SYN, UF9 term.15.
Vertical Ramp Reset from V SYN, UF9 term.11.

The Horizontal Drive signal timing is determined by the D2 output of CPU & Horizontal Decoder UF8 and by monostable multivibrator UG4. When D2 goes low, the Horizontal Drive goes high as a result of this low at the terminal 4 Preset input to the flip-flop in UG2. When D2 goes from low to high, it starts the timing of the one-shot in UG4, which applies a high at the terminal 2 D input of the flip-flop in UG2. The high at UG2-4 causes the flip-flop to follow its D input on the positive-going transitions of the terminal 3 Clock input. So there is no immediate change in the Horizontal Drive signal -- it remains high. When the one-shot in UG4 times out (this time is adjustable by R20), the D input to the flip-flop goes low. Horizontal Drive goes low on the next positive-going Clock transition (the HØ Character Counter output of the 5027 CRT Controller). This is the Horizontal Drive signal used in the Analog Board.



E. VIDEO BOARD

The Video Driver Board is mounted at the rear of the CRT by mating its socket to the CRT pins. It contains the three video drivers, three bias adjustment potentiometers and the socket for connections to the CRT. The circuit is shown on Schematic Drawing 100896.

Video Amplifiers are driven by signals from the Logic Board connected through J2. The signals for red, green and blue are passed through 74S37 gates UA1 to three identical driver transistors Q1, Q2 and Q3 (Q4, Q1 and Q7 in older boards). At the gate inputs resistors R19, R20 and R21 and diodes CR8 through CR13 help prevent transients resulting from CRT arcing from passing back to the Logic Board. The second input of the three gates is +5V. The 4th gate in UA1 is not used. Power for the gates is +5V regulated from the Analog Board, connected to UA1 terminal 14. A 1N4735 zener diode prevents the +5V supply from exceeding 6.2volts in case of regulator failure.

In the Red Drive circuit, transistor Q1 is a common-base amplifier. Its emitter is driven by the signal from UA1-3. The emitter bias is from the +5V Regulated and the collector supply from the -48V Regulated on the Analog Board, both connected through J1. The collector load includes frequency compensation to obtain the required bandwidth. Diodes CR1 and CR3 reduce the effect of CRT arcing. The Green and Blue circuits are similar. The driver outputs are connected through 1000-ohm series resistors (470 ohms in older units) and socket S1 to the CRT Red, Green and Blue control grids.

Screen Control Potentiometers R1, R2 and R3 provide individual bias adjustment for the Red, Green and Blue CRT Screen grids to control brightness and color mix. +200 VDC is supplied to three potentiometers via J1 from a rectifier associated with the horizontal sweep portion of the Analog Board.

6.3 VAC for the CRT socket filament connections is from transformer T1 on the Power Board, connected through J1.

Focus voltage for pin 9 of the CRT socket comes through a separate HV lead with a connector to mate with the Focus lead of the HV Rectifier(attached to the Analog Board).

Cathode return for all three guns is to ground through R6 (10K).

Grounding connection for CRT socket terminal 10 and the tube mounting springs is to frame ground.

A typical video waveform at the collector of Q1 has an amplitude of approximately 40 volts p-p. The waveforms at UA-1, UA1-3 and Q1-e are approximately 4 volts p-p.

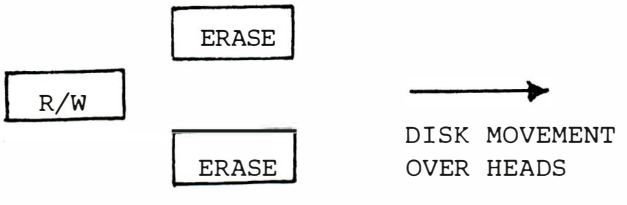
F. DISK DRIVE

The Floppy Disk Drive uses the standard 5 1/4" diskette package. Each of 40 tracks used for data(of 41 total tracks) is treated as consisting of 10 sectors with 128 bytes each--about 1280 bytes per track, including formatting information, or 51,200 bytes per diskette. The home "zero" track (outer most track) is not used for data. Compucolor II has provision for use of two floppy disk drives. The basic set includes one drive mounted in the right front of the cabinet. An optional external second disk drive can be connected to a branched Keyboard cable.

The rugged framework contains a DC drive motor which spins a diskette at approximately 300 RPM. A magnetic read/write head and an erase head are mounted on a slide mechanism which a 3-phase motor moves in and out across the recording tracks in 40 incremental steps. The Disk Controller Board, mounted on the disk drive framework, contains the record/reproduce amplifiers, drive motor speed control circuit, stepper motor drives, and control circuitry. The built-in disk drive is connected to the Logic Board by a flexible cable. Read and Write data are transferred to and from the Logic Board in serial form. Control data for the drive assembly is the 8-bit parallel output of the 5501 I/O Device (through an octal buffer) on the Logic Board. Bits Ø-2 control the stepper motor, one of bits 4 or 5 controls the drive select, and bit 3 determines Write or Read. (Bits 6 and 7 are not used in the Disk Drive at present.)

The upper portion of Schematic Drawing 100873 shows the Reproduce Amplifier. Signals induced in the R/W Head by the diskette magnetic fields are connected through a filter and clipping circuit to one section of Dual Preamplifier UB2. Negative feedback is provided through R19 and amplifier phase compensation by R24-C4. The reproduce signal is carried through emitter-follower transistor Q1 and a noise reduction coupling circuit to the second section of UB2. (CR9 and CR10 block the center portion of the signal and most of the noise.) Negative feedback for the first section also is through a T-pad (R52,R53,C27). Section two has diodes CR3, CR4, CR7 and CR8 across R25 for output clipping. R27-C6 provide phase compensation. Operational amplifier UB3, functioning like a trigger, latches the signal to a section of inverting octal buffer UA2. (See waveforms shown on Schematic Drawing 100873. The waveform shown for TP3 is inverted by UA2 and then inverted again by the line receiver in the Logic Board to be compatible with positive logic.)

Serial data to the Record Amplifier is passed through sections of inverting Octal Buffer UA2 to drive two transistors in Transistor Array UB1. When these transistors are enabled, their output drives the R/W Head to record data magnetically on the diskette. Current through the Erase Head keeps the width of the track within limits by erasing any portions that extend beyond the specified track width, (see sketch of head arrangement). Effectively, only the transitions are recorded. The original signal is recovered by the reproduce amplifier as described above.



HEAD ALIGNMENT

Control of the Record Amplifier is by bit 3 from the output of the Logic Board's 5501 I/O Controller. When WRITE is low (and the SELECT bit also low), it is passed through two sections of inverting Octal Buffer UA2 in

series to be a low at UB1 terminal 12 and enable the Record Amplifier. (The low turns off transistor 14-12-13. The resulting high at term 4 turns on transistor 5-4-3 to pass the emitter current of the record amplifier transistors immediately above.)

The high at UA2-17, which is a result of a WRITE low, turns on a high-current Darlington in UA3 to pass current through the Erase Head to control the track record width.

The Disk Drive Motor speed is controlled by UA4 and associated circuitry. The transistor shown near the right edge of the UA4 block passes the drive motor current. The two transistors immediately to its left control its conduction. When the SELECT bit (bit 4 for the built-in disk drive or bit 5 for the optional added disk drive) is high, the 3-14 section of UA3 conducts to present a low at terminal 11 of UA4 and prevent current flow through the drive motor. A SELECT low results in a high at terminal 11 to allow current flow through the motor. The output of the comparator in UA4 then controls the conduction of the control transistors. This is determined in part by the adjustment of R10 and in part by the output of the Pulse Generator. A tachometer attached to the drive motor (connected to UA4 terminals 3 & 4) and the pulse timing components R8-C2 control the Pulse Generator output. If the drive motor speed becomes too high, the higher tachometer output operates through the Pulse Generator and comparator to reduce conduction through the control transistors and reduce motor current.

Too slow a drive motor speed results in lower tachometer output, which serves to allow increased current through the drive motor. Disk drive speed is set for 300 RPM by adjustment of R10. If the motor should stall, the Stall Timer portion of UA3 prevents high motor current for any extended period of time.

The Stepper Motor moves the R/W Head and Erase Heads across the diskette one track at a time under control of bits Ø-2. A low at any bit results in a high out of the inverting Octal Buffer section in UA2 to turn on the associated Darlington in UA3.

The SELECT bit also is connected to the Octal Buffer gates (UA2 terminals 1 and 19). When the SELECT bit is high it gates all of the buffer sections into the high-impedance state to prevent passage of serial data in or out and operation of the stepper motor. 74LS138 (not in earlier models) allows passage of only one low bit at a time to UA2.

This gating also prevents flow of recording current. The SELECT high on the gate A of UA2 section 2-3, causes a high at terminal 12 of UB1. Transistor section 14-12-13 turns on to cause a low at terminal 4, turning off transistor section 5-4-3 to block emitter current from the record amplifier transistors above. Thus all functions of the disk drive assembly are disabled until a low SELECT bit commands the drive motor to start.

G. KEYBOARD

Compucolor II has a detachable keyboard which is available in several models. It is connected to Logic Board connector J1, through the cabinet

rear cover. There are four parallel input lines and 12 parallel output lines, plus a CPU reset line, +5V and ground.

Schematic Drawing 100878 shows most of the Keyboard wiring as a matrix. The four input lines (connector terminals 3,2,5 and 4 in the upper left corner of the diagram) bring series of data bits 0Ø-03 from the Logic Board's 5501 I/O Controller to the 74159 4-line-to-16-line Decoder in the Keyboard. The 74159 decodes the four binary bits into 16 mutally exclusive codes, Ø-15, for the horizontal lines of the matrix. The seven vertical lines of the matrix are connected through 2,200-ohm resistors to +5V. Thus all seven matrix output lines (bottom of the schematic) are high except when key closure connects a pattern of lows from the 74159 Decoder. This coded pattern is the input presented to the Logic Board.

The remaining five lines of the Keyboard's 12-line output (shown in the lower right portion of the drawing) also are connected to +5V through resistors. The five outputs are high except when the associated key is closed to give a low. The Reset key (drawing lower right) applies a low to the Logic Board's 8224 Clock Generator RESIN input. This results in a RESET to the 8080 CPU to force it back to its initial condition -- the condition initialized when the Compucolor II is turned on.

An optional branched connector cable permits connection of an add-on Disk Drive as well as the Keyboard. Keyboard functions remain the same in this configuration.

H. ADD-ON PROM

The plug-in Add-On PROM has four IC's mounted on a printed circuit board 4.25x2.07 inches. It is available as 4K, 8K or 16K.

Capacity	IC Type	
4K	2708 EPROM	1024x8
8K	2716 EPROM	2048x8
8K	9216 MASK ROM	2048x8
16K	4732 MASK ROM	4096x8

Several connections are dependent upon the type of IC used. Terminals for appropriate strapping are mounted on the board.

	INPUT →	+12	-5	A12	A10			CS		GND	A11
	PATCH NO. →	1	2	3	4	5	6	7	8	9	10
ROM CHIP	2708	X	X					X		X	
	2716	X	X				X		X		
	4732					X		X			X
	9216	X			X			X		X	
	36000			X		X		X			X

Capacitors for power source by-passing are included. Connectors at each end of the board mate with two J9 connectors on the Logic Board. Note that the end terminals 1 through 14 mate with the connector nearest the edge of the Logic Board. Power must be OFF when the Add-On PROM is mated with the Logic Board.

Up to 12 address bits are received from the Address Bus. The 8-bit output is connected to the External Data Bus. Chip Select is determined by the ROM/PROM Decoder (UB3) on the Logic Board.

I. ADD-ON RAM

The plug-in Add-On RAM has eight one-bit-wide dynamic RAM chips mounted on a printed circuit board. It is available as 16K, with 4116 type IC's.

Capacitors for power source by-passing are included. Connectors at each end of the board mate with the two J8 connectors on the Logic Board. Note that the end with terminals 1 through 12 mates with the connector nearest the edge of the Logic Board. Power must be OFF when the Add-On RAM is mated with the Logic Board.

The Add-On RAM is addressed through the 3242 Address Multiplexer/Refresh Counter (UA3) in parallel with the resident RAM. The output of the RAM Address Decoder (UE2) provides the $\overline{\text{Row Address}}$ and the Column Address $\overline{\text{Strobes}}$ to the External Data Bus in parallel with the resident RAM. The MW signal from the Bus Driver/Controller (UB2) indicates whether data on the Data Bus is to be written into memory or data in memory is to be read onto the Data Bus.

VI. MAINTENANCE

General

This section contains information required for maintenance of the Compucolor II. It covers preventive maintenance, adjustment procedures, trouble-shooting sugguestions and parts replacement instructions.

A thorough understanding of the system and sub-assembly descriptive material, including the drawings, is essential for effective maintenance.

Safety Precautions

1. HAZARDOUS VOLTAGES are present within the Compucolor II. When the rear cover is removed for adjustments and/or trouble-shooting, exercise CAUTION especially to AVOID CONTACT WITH THE CRT HIGH VOLTAGES, THE INPUT 115 VAC, AND NUMEROUS CIRCUITS IN THE POWER, ANALOG AND VIDEO BOARDS HAVING 150 VDC AND HIGHER.

2. Do not remove, install or handle the picture tube in any manner unless shatterproof goggles are worn. Persons not so equipped should be kept away while picture tubes are being handled. Keep the picture tube away from the body while handling.

3. Always use the manufacturer's recommended replacement components when replacing parts, especially in the Analog Board circuits associated with the cathode ray tube. Use of the correct parts is an essential step in keeping X-Radiation at a minimum.

   The only source of X-Radiation in the Compucolor II is the picture tube. The cathode ray tube used is specifically constructed to limit X-Radiation. For continued X-Radiation protection, the replacement tube must be the same type as the original, including suffix letter, or a Compucolor Corporation approved type.

   The CRT high voltage must be maintained within specified limits. The high voltage must never, under any circumstances, exceed 25 KV. The usual value is near 20 KV.

4. A further caution:

   Part of the Compucolor II circuitry on the Power and Analog Boards is not referenced directly to frame ground. The rectifier for 150 VDC is connected to the 115VAC line, so the 150-volt supply and all circuits directly supplied by it have a "hot" common lead, several volts from frame ground. Any instrumentation to be connected across these circuits must be floating --- neither side grounded.

Servicing Precautions

1. Observe original lead dress, particularly in high voltage and video areas.

2. Always connect the common lead of a test instrument to the circuit before connecting the positive lead; conversely, always remove the common lead of a test instrument last.

3. Do not check for high voltage by drawing an arc. Use a high voltage meter or a high voltage probe with a VOM.

4. Do not bridge electrolytic or other large value capacitors into a live circuit since resultant surges may damage solid state devices.

5. Some transistors are equipped with heat sinks. Do not operate the transistor with the heat sink removed.

6. All soldering irons used where transistors and integrated chips are concerned should be 35 watt irons and ungrounded so that no voltage will be applied to the solid state device during the soldering operation. This precaution is to prevent possible damage to the device due to excessive heat or voltage applied under no bias conditions.

Instrumentation

Performance of maintenance procedures requires a multiple trace oscilloscope with a bandwidth of 15 Mhz., a digital logic probe and a VOM. The VOM must have a high voltage probe or a separate high voltage meter must be used for measuring the CRT voltage (up to 25 KV). (Remember to "float" the oscilloscope and any electronic VOM before connecting to certain circuits in the Analog and Power Boards.)

Preventive Maintenance

The Compucolor II requires a minimum of preventive maintenance: periodic cleaning of the outside surfaces of the equipment may be performed, along with checks of the condition of the interunit cabling and internal components of the chassis. To clean the CRT screen, display enclosure and keyboard use a lightly moistened lint-free cloth or vacuum cleaner. A mild household cleaner can be used to clean the outside surfaces of the cabinet and keyboard. Most of the circuit boards in the display unit and keyboard operate at low power levels. Consequently their contacts are sensitive to dust, oil, moisture, and corrosion. When the circuit cards are removed, the contacts should be cleaned before re-inserting. Use a lint-free cloth moistened with trichloroethlylene or another suitable solvent; then remove the film left by the cleaning fluid.

Cabinet Disassembly

The Compucolor II cabinet must be partially disassembled for most alignment and trouble-shooting. Care must be exercised to avoid damage to the Logic Board and Video Board during removal of the rear cover. With power off, disconnect the keyboard and any external additions connected to the rear edge of the Logic Board.

Remove the four screws (3 top, 1 bottom) that fasten the rear cover to the front portion of the cabinet. Then, with the cabinet upright on the bench, slide the rear section back slowly to allow the Logic Board to drop gently from its retaining slots in the front and rear sections. This procedure also avoids rear cover contact with the Video Board mounted on the back of the cathode ray tube. The keyboard now may be reconnected and power applied to the unit. Normal alignment procedures require no further disassembly.

Trouble-shooting and/or repair likely will require further disassembly. Power should be off when interunit cables are to be disconnected.

Video Board - Circuit measurement points are readily accessible with the board in place. If component replacement or other repair is indicated, disconnect the cables to the Analog and Digital Boards; carefully disengage the Video Board from the CRT.

Analog Board - Measurements required during alignment may be performed with the Analog Board in place. Further access likely will be required during trouble-shooting. Remove three mounting screws (one bottom, one at lower left and well into the forward section of the cabinet, and one at the top). Then the unit can be moved enough to make its components somewhat more accessible. For complete removal, first disconnect all cables to and from the board.

Power Board - Disconnect the power cord and the internal cable to the Analog Board. Remove two mounting screws from the exterior side of the rear cover.

Disk Drive - Disconnect the cable from the Logic Board. The unit is fairly heavy relative to its small size. It should be supported by hand carefully to avoid damage to the circuit board during removal. Remove the Phillips head screw from the bracket strip just above the drive assembly, as viewed from the rear. Tilt the rear of the drive unit up a bit and lift the entire assembly slightly to free the two tabs securing the lower front of the drive assembly. Remove the Disk Drive through the front of the cabinet.

Alignment

Perform all adjustment procedures with the input power at 115 VAC.

Regulated Voltages: Using a DC Voltmeter with an accuracy within 2% at 5 volts, check voltage between Logic J6-4 and frame ground. If not 5.0 ± 0.1 volts, adjust R22 to obtain an indication of 5.0 VDC. After this adjustment has been made, the voltages between the following points and ground should be as indicated:

From Analog	To	DC Voltage
E23	Ground	-5.0 ± 0.3
E20	Ground	-12.0 ± 0.6
E19	Ground	+12.0 ± 0.6
E16	Ground	-48.0 ± 2.0

Noise and ripple, as viewed on an oscilloscope will vary with the type of operation but should not exceed 3% peak-to-peak at any of these points.

Vertical Deflection: Erase the screen with a background color other than black.

1. Operate the "BG ON" key.
2. With "CONTROL" key depressed, strike a color key (e.g., "Q" for red).
3. Strike the "ERASE PAGE" key.

On the Analog Board, adjust VERT HEIGHT R106 and VERT CENT R105 for a pattern height of approximately 6¾ inches, centered vertically on the screen.

Horizontal Deflection: Adjust HOR WIDTH R109 on the Analog Board for a pattern width of 9 3/8 inches. Then fill the screen with a pattern of white dots on a black background.

1. Operate the "BG ON" key.
2. With "CONTROL" key depressed, strike the black color key "P".
3. Then, strike the "FG ON" key.
4. With "CONTROL" key depressed, strike the white color key "W".
5. Strike the "(ESC)" key, "Y" key and "." key in succession.

On the Digital Board, near corner by keyboard cable, adjust R20 to center the pattern horizontally. Note that the pattern moves in discrete two-character jumps. Adjust the pot by touch to be half-way between two jump points.

Focus: With the pattern of dots still filling the screen, adjust the FOCUS potentiometer, mounted on the rear edge of the Analog Board frame, for optimum focus over the entire screen. (When the cabinet is fully assembled, a hole at the rear provides access to the FOCUS control.)

Purity: With the pattern of white dots still on the screen, note the convergence adjustment condition -- the dots in the center should appear white, with little or no color-tinged edges. If the convergence adjustment appears reasonably good, proceed with the purity adjustment. Otherwise, first follow the convergence procedure detailed later in this section, even though parts of it will have to be repeated.

Erase the screen with background color Red (keyboard operation described under Vertical Deflection adjustment.) Purity adjustment is needed if the entire pattern is not a uniformly red color.

The Compucolor II should always be facing either north or south during purity adjustment. This assures that any effect of the earth's normal magnetic field upon beam landing will be negligible when the unit is placed in its normal viewing location.

The unit should be at room temperature (60°F or above) for at least 30 minutes before adjustments are made. It should be in operation for at least 10 minutes before attempting purity or convergence adjustemnts.

Degaussing may be required. Move a manual degaussing coil (GC 9317 or equivalent) slowly around the unit and back and forth in front of the picture tube. Withdraw the coil slowly to a distance of at least six feet before disconnecting the coil from its AC power source.

1. With the screen still erased with the background color Red, loosen the yoke clamp and move the yoke to the rear as far as possible.

2. Rotate the purity rings by the two adjustment tabs (on rectangular magnet assembly just behind yoke) to obtain a clean red area at the center of the CRT screen.

3. Push yoke forward until a uniform red raster is obtained. The raster should be slightly larger than 6 by 9 inches and not rotated from the horizontal orientation. Tighten the yoke clamp.

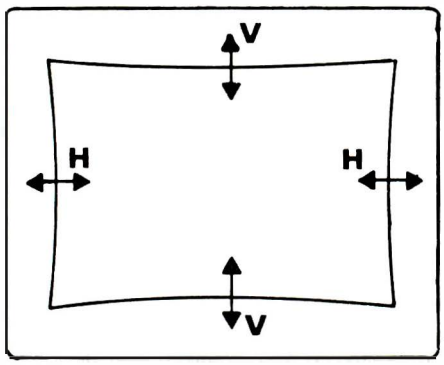
4. Erase the screen with the background color white. The raster should be uniformly white. It may be necessary to reconverge the center of the screen by adjustment of the red and blue horizontal and vertical thumbwheels on the rectangular magnet assembly. The Color Temperature and Brightness procedure (immediately following) may also be required.

5. If the central area of the screen is not uniformly white, repeat the purity adjustment and the red and blue convergence adjustments. (Other adjustments, performed a bit later, take care of convergence at top, bottom and sides.)

Color Temperature and Brightness: Fill the screen with white characters on a black background. (The procedure is the same as that outlined in the Horizontal Deflection paragraphs.)

On the Video Board, turn the three screen grid controls R1 (Red), R2 (Green) and R3 (Blue) fully CCW. Turn the RED control R1 clockwise until the red vertical retrace raster line at the top of the screen is barely visible; then return it CCW slightly to render the retrace invisible. Adjust GREEN control R2 and BLUE control R3 in similar fashion. Carefully touch up the adjustment of the three controls to obtain white letters with brightness at a comfortable viewing level.

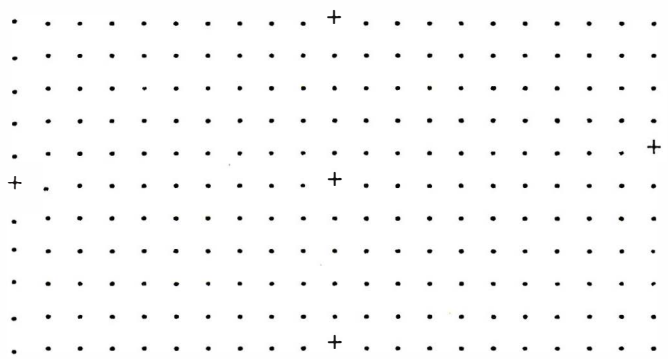
Pincushion: With the screen still filled with a pattern of letters, note whether top and bottom lines are straight horizontally. Adjust VERT PINCUSHION R107 on the Analog Board to obtain straight lines horizontally (see sketch). For straight lines vertically at the left and right sides, adjust HOR PINCUSHION R108. (R108 omitted in early models.)



V = Vertical Pincushion R107

H = Horizontal Pincushion R108

Convergence: Fill the screen with the convergence test pattern of dots and five "+" symbols.



1) Operate the "CPU RESET" key, then the "BG ON" key.

2) With "CONTROL" key depressed, strike the black color key "P".

3) Strike the "FG ON" key.

4) With "CONTROL" key depressed, operate the white color key "W".

5) Operate the "(ESC)" key, "Y" key and "." key in succession.

6) Then operate "(ESC)" and "X" (for page mode).

7) Operate the "HOME" key, then the "↓" key 16 times and the "←" key once.

8) With the "SHIFT" key depressed, strike the "+" key two times. ("+" symbols should appear center right and center left.)

9) Operate the "TAB" key four times to move the cursor to screen center. Enter "+".

10) Operate "↓" key 15 times and the "←" key once to bring the cursor to bottom center. Enter "+".

11) Operate "↓" and "←" once each to move the cursor to top center. Enter "+".

12) Operate "HOME" key to return cursor to upper left.

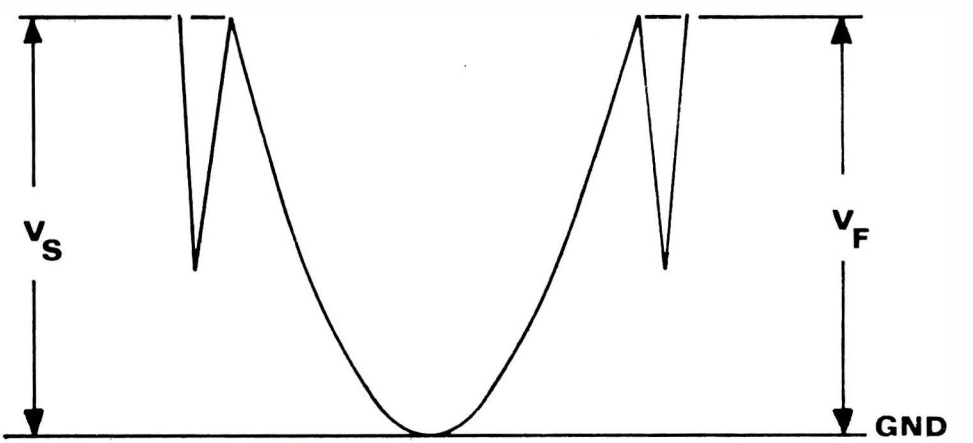
If the Focus and Purity adjustments have been performed correctly, the center "+" should be a well-defined white symbol.

On the Analog Board, adjust TOP R96 for best convergence at the top "+" (white symbol without color-tinged edges). Repeat with BOTTOM R97, RIGHT R95 and LEFT R94 for best convergence in the bottom, right and left areas of the screen.

If any of the last four potentiometers reach the end of the adjustment range before satisfactory convergence is achieved, proceed as follows:

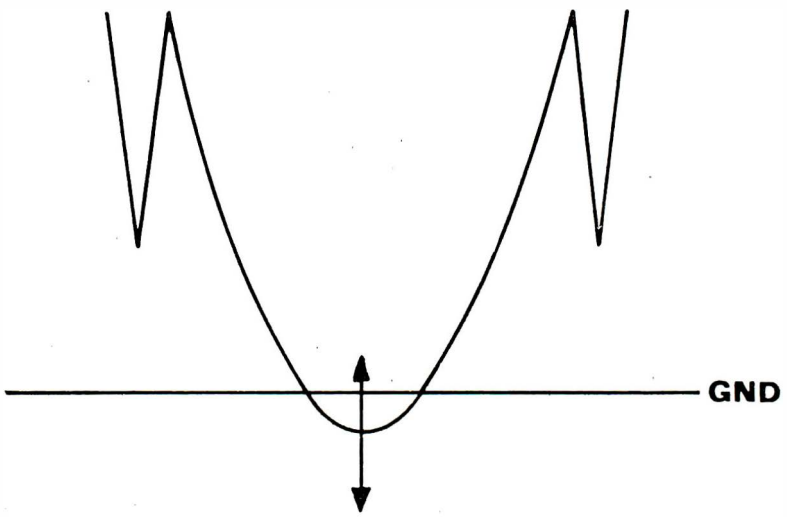
1) Return the four potentiometers to the center of their adjustment range.

2) With the oscilloscope, monitor the Horizontal Parabola pattern at U17-3 on the Analog Board. Adjust R102 to equalize the height of the end points of the parabola.



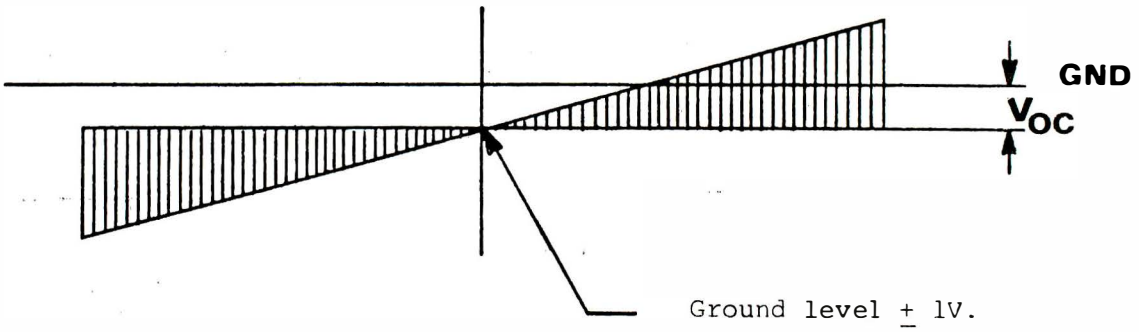
Make $V_s = V_f$

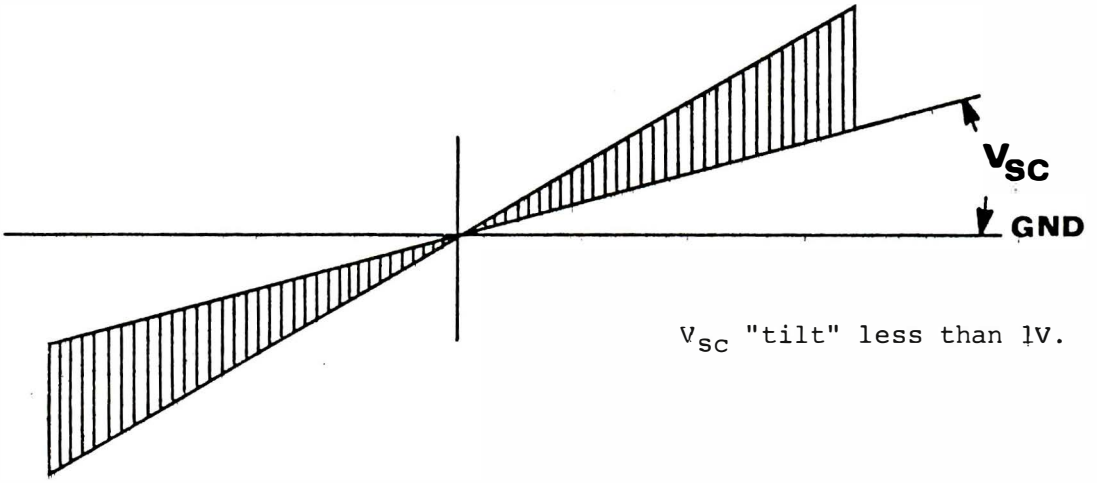
Then adjust R101 to bring the bottom of the parabola to Ground Level.



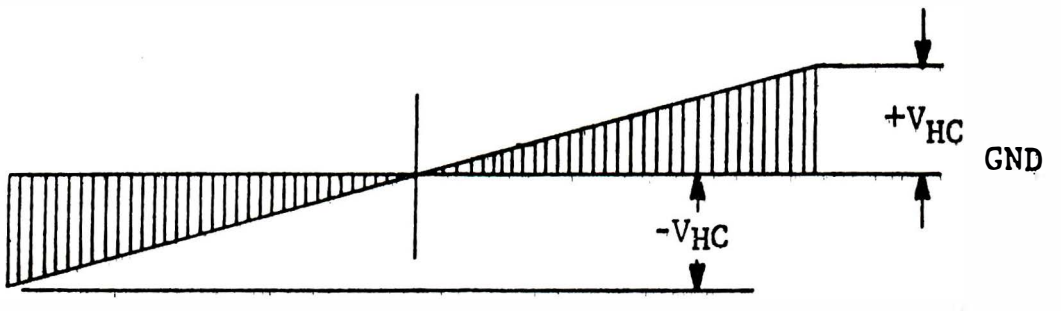
3) Monitor the Vertical Parabola pattern at U11-3 and adjust R103 and R104 in similar fashion.

4) Monitor the Pincushion pattern at U16-3. The center of the pattern should be at Ground Level, the baseline horizontal and the right and left end points equal in height.



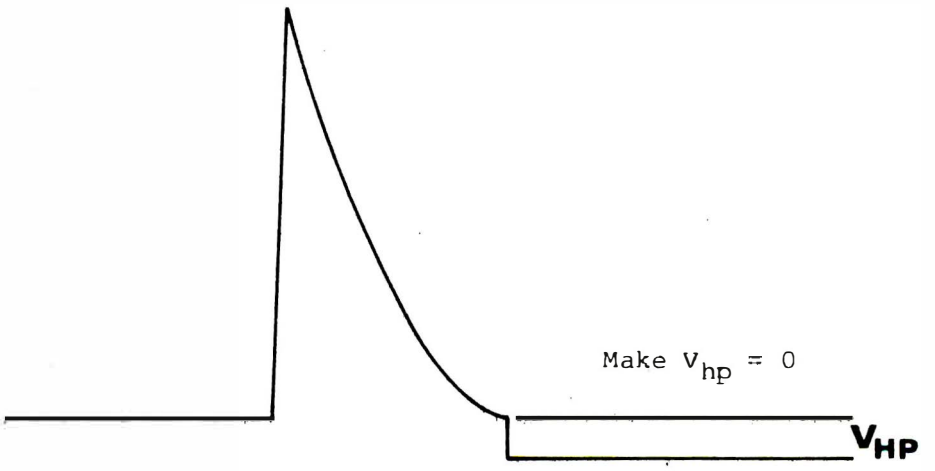


V_{SC} "tilt" less than 1V.

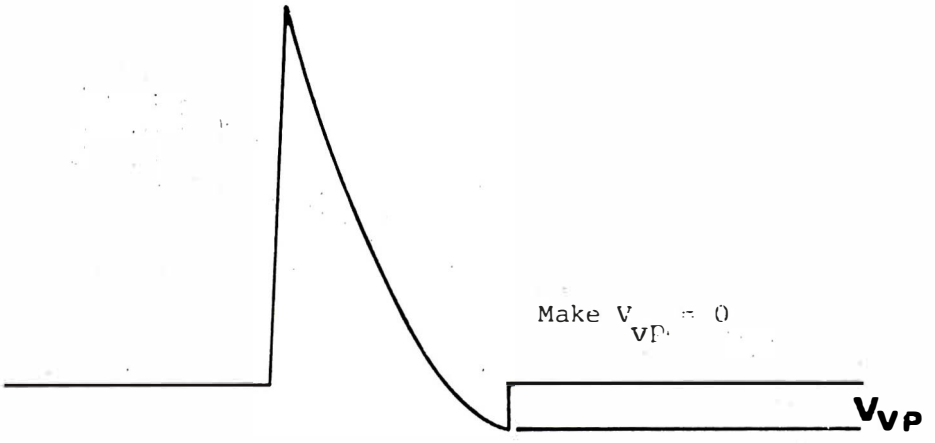


Height of pattern end points within 1V. of equal.

5) Monitor pattern at U5-1 and touch up R101 adjustment to eliminate any remaining offset.



6) Monitor pattern at U5-8 and touch up R104 adjustment for zero offset.



It should now be possible to obtain convergence in all areas of the screen. Adjust R96, R97, R95 and R94 for best convergence in the top, bottom, right and left areas of the screen. Then touch up adjustments, observing the SAME ORDER of potentiometer adjustment.

DISK DRIVE: The Disk Drive Assembly has a strobe disk (on the side nearest the CRT) for speed check. While viewing the strobe disk under 60 Hz. fluorescent light, strike the keyboard "AUTO" key to cause the drive to run. (Note 1: Be sure there is no diskette in the unit.)

While the drive is running, the outer pattern on the strobe disc should appear very nearly stationary. If the pattern drifts appreciably in either direction, adjust R10 on the Disk Controler Board to "stop" the pattern. It probably is best to remove the Disk Drive from the Compucolor II cabinet to make this adjustment.

(Note 2: It is necessary to strike the "RESET" key to stop the drive.)

(Note 3: If the Compucolor II is powered by 50 Hz. 115 VAC, perform the adjustment under 50 Hz. illumination and observe the inner pattern on the strobe disk.)

TROUBLE-SHOOTING

In system-level trouble-shooting the object is isolation of one major board or assembly as the cause of the malfunction. One method of doing this is substitution of major assemblies. Always turn power off when removing or replacing any assembly or component. Refer to disassembly procedures described earlier in this section.

In addition, some deductive reasoning may be performed by observing the CRT display screen under various system operating conditions. Information contained in the system and subassembly description sections can be helpful in signal tracing and trouble analysis.

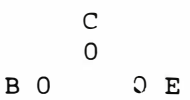
The extent to which individual part replacement may be efficient is dependent upon the user-skill level. Establishment of a maintenance policy is suggested--e.g., "Attempt repair of Analog Board; return malfunctioning Digital Board to Compucolor Corporation.

TROUBLE-SHOOTING TECHNIQUES

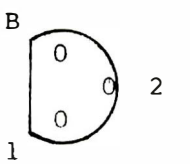
1. Check to see that all plugs and connectors are properly connected.
2. Make a visual check for broken connection or damaged components.
3. Check for any blown fuses.
4. If there is a convergence problem, see if it can be corrected by alignment. See section on Alignment.
5. Always check low voltage power supplies before beginning other trouble shooting.
6. Note symptoms and refer to block diagram and schematics.
7. Locate the circuit area in which the problem is believed to be contained.
8. Read circuit description of suspected circuit.
9. Follow check out procedure until defective component or components are found.

TRANSISTOR CONNECTIONS

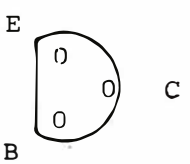
All connections are shown as viewed on the component side of the printed wiring board.



Analog Board: Q1, Q2, Q5, Q6, Q7
(Power transistors mounted on the Analog Board wrap connect into the component side of the board as indicated at left.)

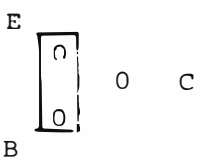


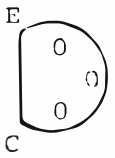
Analog Board: Q13, Q15
(FET E111)



or

Analog Board: Q3, Q4, Q8, Q17, Q18, Q19

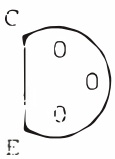




Power Board: Q1

Analog Board: Q9, Q10, Q11, Q12, Q14

Logic Board: Q1, Q2



Video Board: Q1, Q4, Q7

Disk Controller: Q1

Operational Test

Within one minute after unit is turned on, the first line of the screen display should be "DISK BASIC 8001 V6.78 COPYRIGHT © BY COMPUCOLOR", in colors against a black background. (Note: It may be necessary to strike the CPU RESET key once or twice).

Erase the screen with the background color Red.

1) Operate the "BG ON" key.
2) With "CONTROL" key depressed, strike the red "Q" key.
3) Operate the "ERASE PAGE" key.

There should be a uniformly red raster a bit larger than 6" x 9" centered on the screen. The top and bottom edges of the display should be straight. The cursor should appear in the upper left corner of the display.

In similar fashion check the colors Green ("R" key), Yellow ("S"), Blue ("T"), Magenta ("U"), Cyan ("V") and finally Black ("P"). (With the screen erased in Black there is, of course, no visible raster. Only the cursor appears).

Fill the screen with a pattern of white letters.

1) Strike the "FG ON" key.
2) With "CONTROL" key depressed, operate the White "W" key.
3) Strike the "(ESC)", "Y" and "T" keys in succession.

The full-screen pattern of letters should be uniformly White.

Operate the "CPU RESET" key. The pattern of letters is erased and the screen displays "COMPUCOLOR II CRT MODE V6.78". The cursor is at the start of the second line.

Verify that the "CAPS LOCK" key is in the depressed position. Then type material using all keys, for example:

THE QUICK BROWN FOX JUMPS OVER THE LAZY DOG'S BACK.(Space) 1234567890.(Space)

[\]^_(TAB)-(TAB)@;:,/(TAB)<?>+*(TAB)NULL!"#$(TAB)%&(=)

(Note: In order to check both "SHIFT" keys, use the right hand key for some characters and the left hand "SHIFT" key for the others).

Depress "REPEAT" and "." keys simultaneously to add 6 or 8 dots. The line of symbols should read:

[\]^_ - @;:,/ <?> +* !"#$ %&(=).....

Verify that the cursor is near the end of the line of symbols. Strike the "ERASE LINE" key. The line of symbols should be erased and the cursor should return to the start of that line.

Operate the "HOME" key. The cursor returns to the upper left corner of the screen. Operate the other cursor control keys to verify that the cursor moves down, right, left and up in accordance with the direction key operated. End with the cursor down a few lines from any material already displayed.

Strike the "A7 ON" key, then the "BLINK ON" key. Then type

BLINK (BL/A7 OFF) TEST

The word "BLINK" is displayed in double height letters and blinks on and off almost two times per second. "TEST" is in normal height letters and does not blink. (Note: In Models 1 and 2, all letters are the same height).

With both "SHIFT" and "CONTROL" keys held down, operate the "CPU RESET" key. The "DISK BASIC" message should appear. Insert the sampler diskette into the disk drive and close door. (See page 2 of the "Instruction Manual"). Depress "AUTO" key. The disk drive runs. A "MENU" or program listing appears on the screen. Strike the "5" key and then the "RETURN ENTER" key. The Compucolor II runs through a memory test, displays "TESTED OK" and then a series of graphic displays follows.

The above test procedure verifies operation of all keys on the standard keyboard and provides a fairly comprehensive test of computer and display functions. Intermittent failures and certain specific problems may require additional testing. Overnight operation prior to final test is recommended.

SECTION VII
COMPUCOLOR II PARTS LIST

VII. COMPUCOLOR II PARTS LIST

Model 3, 4 and 5 Assemblies

ITEM	CCII NO.	QUAN.	DESCRIPTION
1	100953	1	Cab. Back. Mod.
2	100954	1	Cab. Front Mod.
3	120084	21	#6 X 3/4 Self Tap
4	900004	1	13" CRT
5	110091	1	CRT Sling
6	900029	2	CRT Spring
7	110092	1	CRT Mtg. Brack.
8	100942	1	Cab. Sup. Brack.
9	101115	1	Yoke Assy.
10	900023	1	Convergence Assy.
11	100973	1	Disk Drive Assy.
12	101107	1	AC Power Assy
13	120010	3	6-32 x 3/8 TP PH
14	101108	1	Analog Assy.
15	***	*	*See Note Below
16	100988	1	Retaining Strip
17	100985	1	Video Driver
18	100996	1	Cover Plate
19	900032	1	Clamps
20	101113	1	Video Gnd. Strap
21	101116	1	Video Sig. Cable
22	101114	1	Analog Strap
23	110089	1	Handle Brk.
24	110088	1	Handle
25	110032	2	Rubber Foot
26	120014	3	8-32 x 1/2 TP
27	110087	4	Pads Adhesive
28	110054	2	Tie Wraps
29	110029	1	Power Cord
30	120079	1	8-32 x 7/8 TP
31	100990	1	Wiring Diagram
32	100995	1	Block Diagram

*** Item 15 is determined by the Model No.:

MODEL	CCII NO.	QUAN.	DESCRIPTION
3	100963	1	Logic Assy. 8K
4	100964	1	Logic Assy. 16K
5	100965	1	Logic Assy. 32K

COMPUCOLOR II

Recommended Spare Parts List

CCII NO.	DESCRIPTION
101107	Power Supply Assy.
101108	Analog Assy.
100963	Logic Assy. 8K
100964	Logic Assy. 16K
100965	Logic Assy. 32K
100986	Add-on RAM Assy.
100895	Video Drive Assy.
100973	Disk Drive Assy., Complete
100872	Disk Controller Board Assy. Only
900004	12VAXP22 CRT
010047	Spare Parts Kit, Analog
010048	Spare Parts Kit, Digital

The above list presumes repair, other than minor, by replacement of major subassemblies, with the faulty subassemblies being returned to Compucolor Corporation for repair and return.

If substantial in-house repair of subassemblies is contemplated, complete parts lists are available. Repair parts not commonly available from electronics supply houses can be ordered from Compucolor Corporation. With the exception of the cathode ray tube, transformers, cabinets and spare parts kits, ordering quantity is ordinarily five and the minimum order total $100.00.

SECTION VIII
COMPUCOLOR II DRAWINGS

REVISIONS						
REV	ZONE	LTR	DESCRIPTION	ECN	DATE	APPROVED
6			REDESIGN	2173	NH12-3-79	
7	A-B6		CHG Q1 (WAS BU500), Q2 (WAS FT410)	2300	NH 8-6-80	

DESIGNATIONS NOT USED:
R3, 5, 10, 37, 40, 41, 48, 49, 52-65, 67, 68, 75, R83, 84, 88, 90-93, 98, 101-105, 107
C5, 18, 20, 21, 23, 25, 29, 33, 43, 44, 46-49 C51-59, 67, 68, 72, 73, 79
CR8, 9, 10, 13, 14, 17, 27
Q11-16
E12, 13, 14

NOTES:
1. ALL CAPACITORS ARE IN MICROFARADS UNLESS OTHERWISE SPECIFIED.
2. ALL RESISTORS ARE IN OHMS 1/4 WATT ±10% UNLESS OTHERWISE SPECIFIED.
3. ALL VALUES PRECEDED BY A + OR - ARE IN VOLTS.

LAST USED
R131
C94
CR32
Q19
UA14
E25

QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION

PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

MATERIAL

FINISH

DO NOT SCALE DRAWING

CONTRACT NO.

APPROVALS	DATE
DRAWN M. E. Harris	12-3-79
CHECKED	
ENGR Jim Fassa	12-4-79

FOR REV 4 PCB (PRELIMINARY)

Intelligent Systems Corp.

SCHEMATIC ANALOG CC II

SIZE	CODE IDENT NO.	DRAWING NO.	REV.
D		100902	7

SCALE ~ SHEET 1 OF 1

50 PIN BUS

ADD ON RAM MEMORY

INPUT →	+12V	-5V	A12	A10		CS		GND	A11	C5
PATCH NO. →	1	2	3	4	5	6	7	8	9	10	11
ROM I C 2708											
2716											
4732											
9216											
36000											

PATCH 11 IN FOR SOCKETS A5 & A7 ONLY

DROPPED:
C6, 18, 19, 20
LAST- C77

DROPPED:
R18, 19, 22
LAST-R30

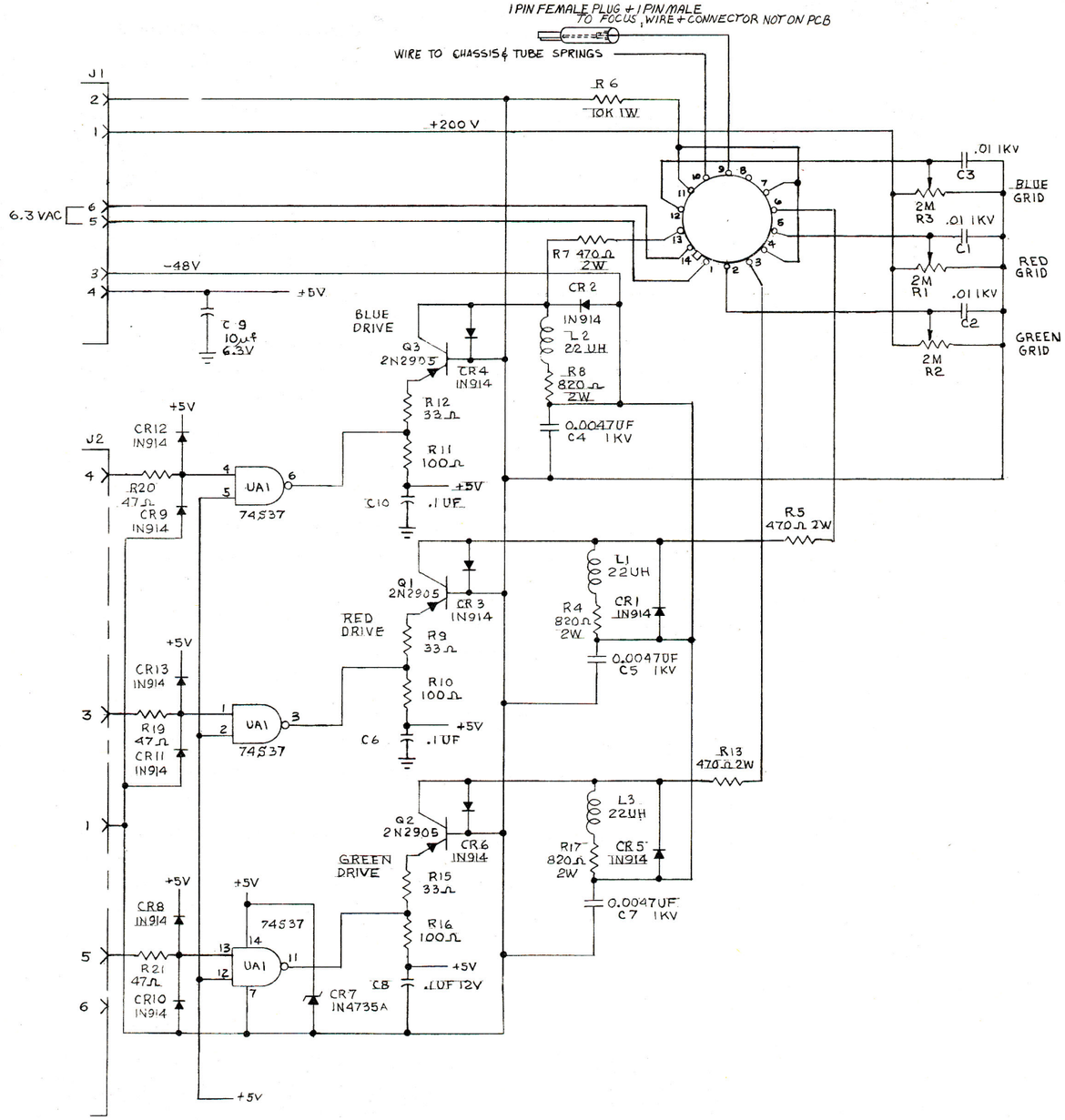
Intelligent Systems Corp.®

	DATE
DRAWN M. E. Harris	9-5-78
CHECKED Jim Tarbell	9-11-78

SCHEMATIC COMPUCOLOR II LOGIC

SIZE	CODE IDENT NO.	DRAWING NO.	REV.
		100961	

REVISIONS					
REV	ZONE	LTR	DESCRIPTION	DATE	APPROVED
1			REDESIGNED J.M.S. 2-21-78		
2			CHG J1 CONN'S, DELETE LEED	5-17-78	
3			REDESIGNED	6-27-78	
4			CHG R23 (WAS 1KΩ) CHG R6, 12, 18 (WERE 47Ω) CHG C19 (WAS 6.8μF) DELETE R 22, C5, 7, 10, 12, 15, 17 & 20) ADD R8, 14 & 20 BY N.E.H.	9-18-78	
5			REDESIGN BY N.E.H.	10-18-78	
6			DELETED R14, 18	10-31-78	



QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION
			PARTS LIST

NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

MATERIAL

FINISH

DO NOT SCALE DRAWING

CONTRACT NO.

APPROVALS	DATE
DRAWN M.E. Harris	10/31/77
CHECKED	

Intelligent Systems Corp.®

SCHEMATIC
VIDEO DRIVER
COMPUCOLOR II 13" CRT

SIZE	CODE IDENT NO.	DRAWING NO.	REV
D		100896-	6

SCALE ~ SHEET OF

100896

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-9745

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED

+5V
C2
C3
25
24
3 00 23 A
2 01 22 B
5 02 21 C
4 03 20 D
UA1
74159
UA2
UA2
UA2
UA2
OPTIONAL PACKAGE 7402
9 06 R2 330Ω +5V
LED CR1
GND 12
10
R1 2.2K
R7 2.2K
0̄ 1̄ 2̄ 3̄ 4̄ 5̄ 6̄ 7̄ 8̄ 9̄ 10̄ 11̄ 12̄ 13̄ 14̄ 15̄
BREAK
INSERT CHAR
DELETE LINE
INSERT LINE
DELETE CHAR
AUTO
HOME
TAB
CURSOR →
CURSOR ↑
CURSOR ←
ERASE LINE
ESC
ERASE PAGE
CURSOR ↓
CARRIAGE RETURN
A7 ON
BLINK A7 OFF
BLACK
RED
GREEN
YELLOW
BLUE
MAGENTA
CYAN
WHITE
BLINK ON
BACKGND ON
FOREGND ON
SPACE BAR
@ A B C D E F G H I J K L M N O
P Q R S T U V W X Y Z [\ ] ^ _
F0 F1 F2 F3 F4 F5 F6 F7 F8 F9 F10 F11 F12 F13 F14 F15
I4 A
I5A
I0 I1 I2 I3
15 14 12 20 18 17 16
+5V
R3 330Ω
CR2 LED
R5 330Ω
CR3 LED
CAPS LOCK
SHIFT
SHIFT
COMMAND
COMMAND
CONTROL
RESET
REPEAT
R1 2.2K
R6 2.2K
R4 2.2K
C1
I7B
I5B
I7A
I4B
I6B
19 21 11 24 26 22

QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION
			PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

MATERIAL

FINISH

NEXT ASSY | USED ON

APPLICATION

DO NOT SCALE DRAWING

CONTRACT NO.

APPROVALS	DATE
DRAWN K.S.H.	9-8-77
CHECKED Stanley Hogan	9-12-78
INKED N.E.H.	5-18-78

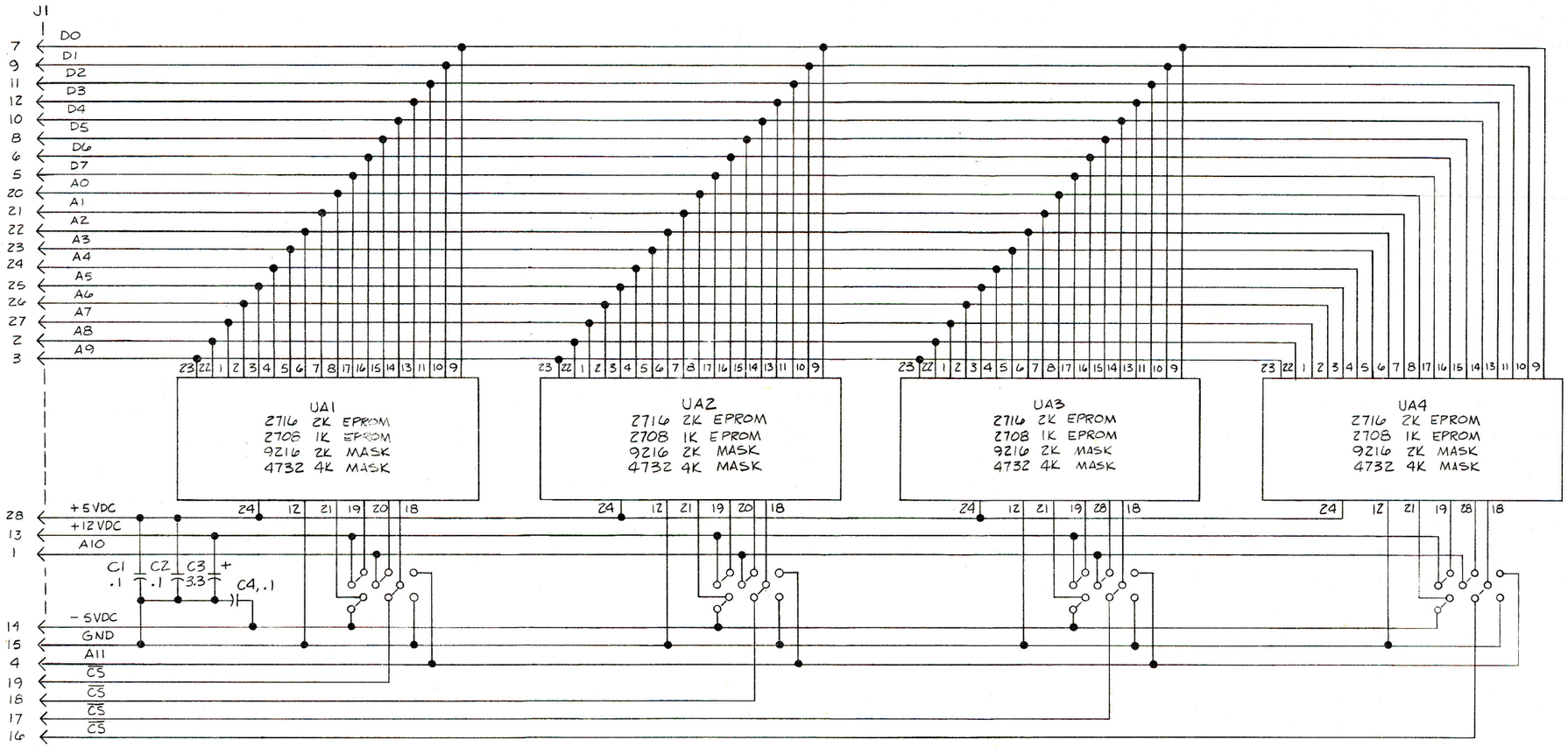
Intelligent Systems Corp.®

KEYBOARD SCHEMATIC

SIZE	CODE IDENT NO.	DRAWING NO.	REV
D		100878	1

SCALE ~ SHEET 1 OF 1

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED



QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION

PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

MATERIAL

FINISH

DO NOT SCALE DRAWING

NEXT ASSY	USED ON
APPLICATION	

CONTRACT NO.

APPROVALS	DATE
DRAWN	8-26-78
CHECKED Stanley Hayami	9-12-78

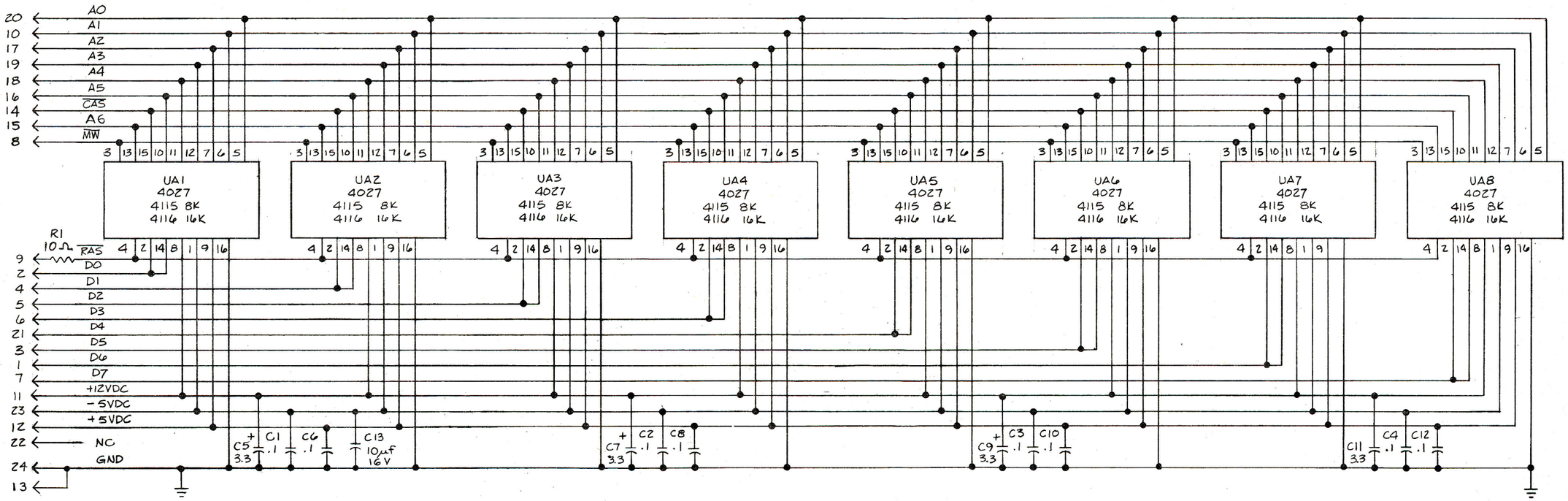
Intelligent Systems Corp.

COMPUCOLOR II ADD ON PROM SCHEMATIC DIAGRAM

SIZE	CODE IDENT NO.	DRAWING NO.
D		100979

SCALE —— SHEET 1 OF 1

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	1	ADD C13 CHG R1 (WAS 47Ω) CHG PIN NOS. 8, 13, 14 + 15	8-28-78	



QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION
			PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

MATERIAL

FINISH

DO NOT SCALE DRAWING

CONTRACT NO.

APPROVALS	DATE
DRAWN	4-26-78
CHECKED	9-12-78

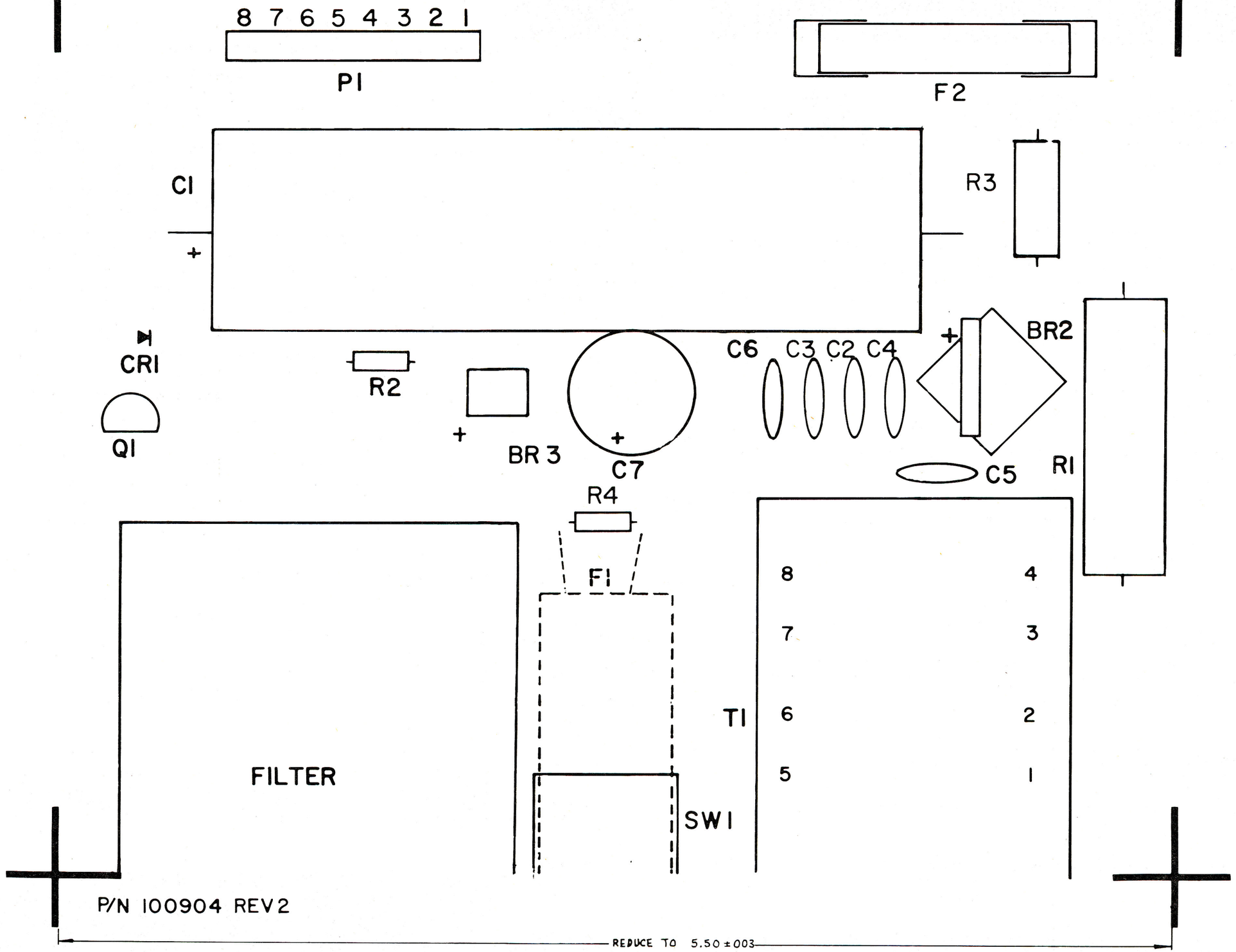
Intelligent Systems Corp.®

COMPUCOLOR II ADD ON RAM SCHEMATIC DIAGRAM

SIZE	CODE IDENT NO.	DRAWING NO.	REV.
D		100984	1

SCALE — SHEET 1 OF 1

NEXT ASSY	USED ON
APPLICATION	

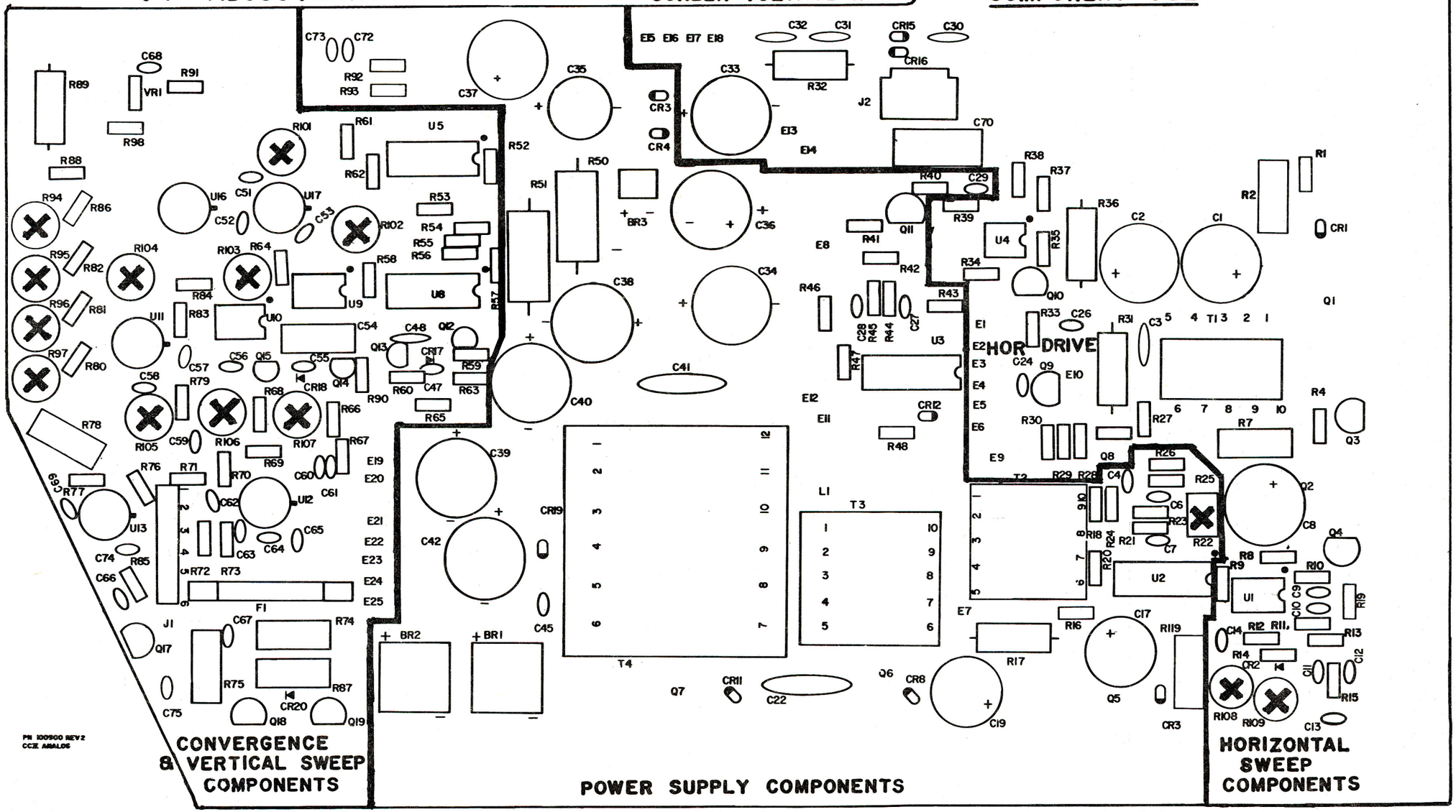

8 7 6 5 4 3 2 1
P1
F2
C1
+
R3
CR1
Q1
R2
BR 3
+
C7
R4
F1
C6
C3
C2
C4
+
BR2
C5
R1
8
7
6
5
4
3
2
1
T1
FILTER
SW1
P/N 100904 REV2
REDUCE TO 5.50 ± 003

ANALOG BOARD

15

✕ = ADJUSTMENT

SCREEN VOLTAGE RECTIFIER COMPONENT SIDE



PN 100900 REV 2
CCE ANALOG

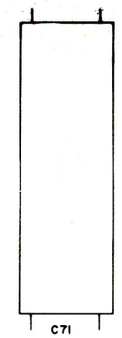
CONVERGENCE & VERTICAL SWEEP COMPONENTS

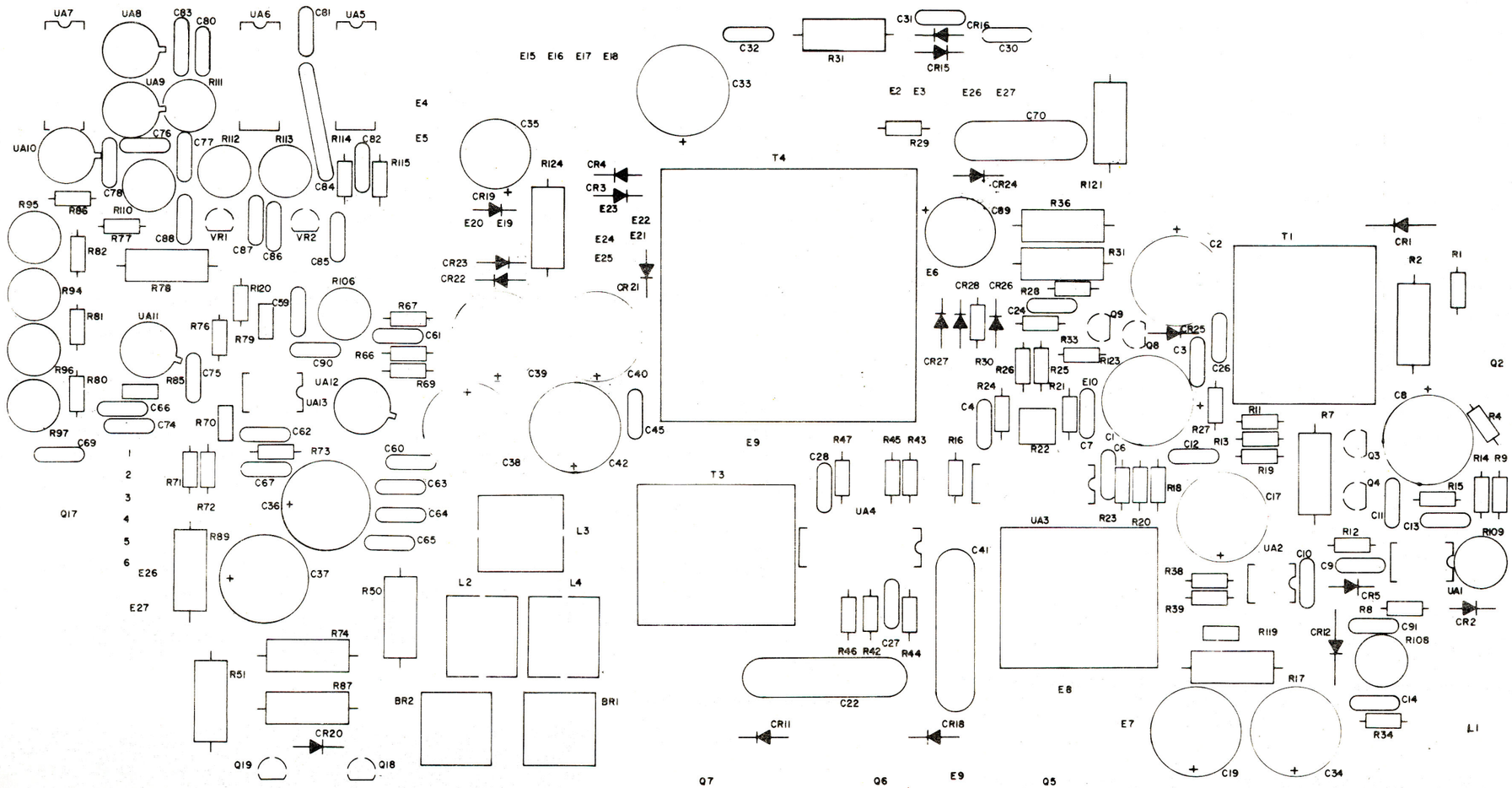
POWER SUPPLY COMPONENTS

HORIZONTAL SWEEP COMPONENTS

PRELIMINARY

Intelligent Systems Corp. ®





ANALOG BOARD

PN.100900 REV. 2

BACK

U1-1
U2-1
Q8
Q10
Q9
U3-1
U8-1
U5-1
Q12
Q13
Q14
U9-1
U17-1
Q15
U10-1
U16-1
U11-1
GND
-48V
+200V
-11V
+11V
Q3
Q4
T1-1
T2-1
T3-1
T4-1
+100V FILTERD
150V
+150V
-12V
+12V
A11-1
+11V
Q18
Q19
Q17
U13-1
J1-1
U12-1

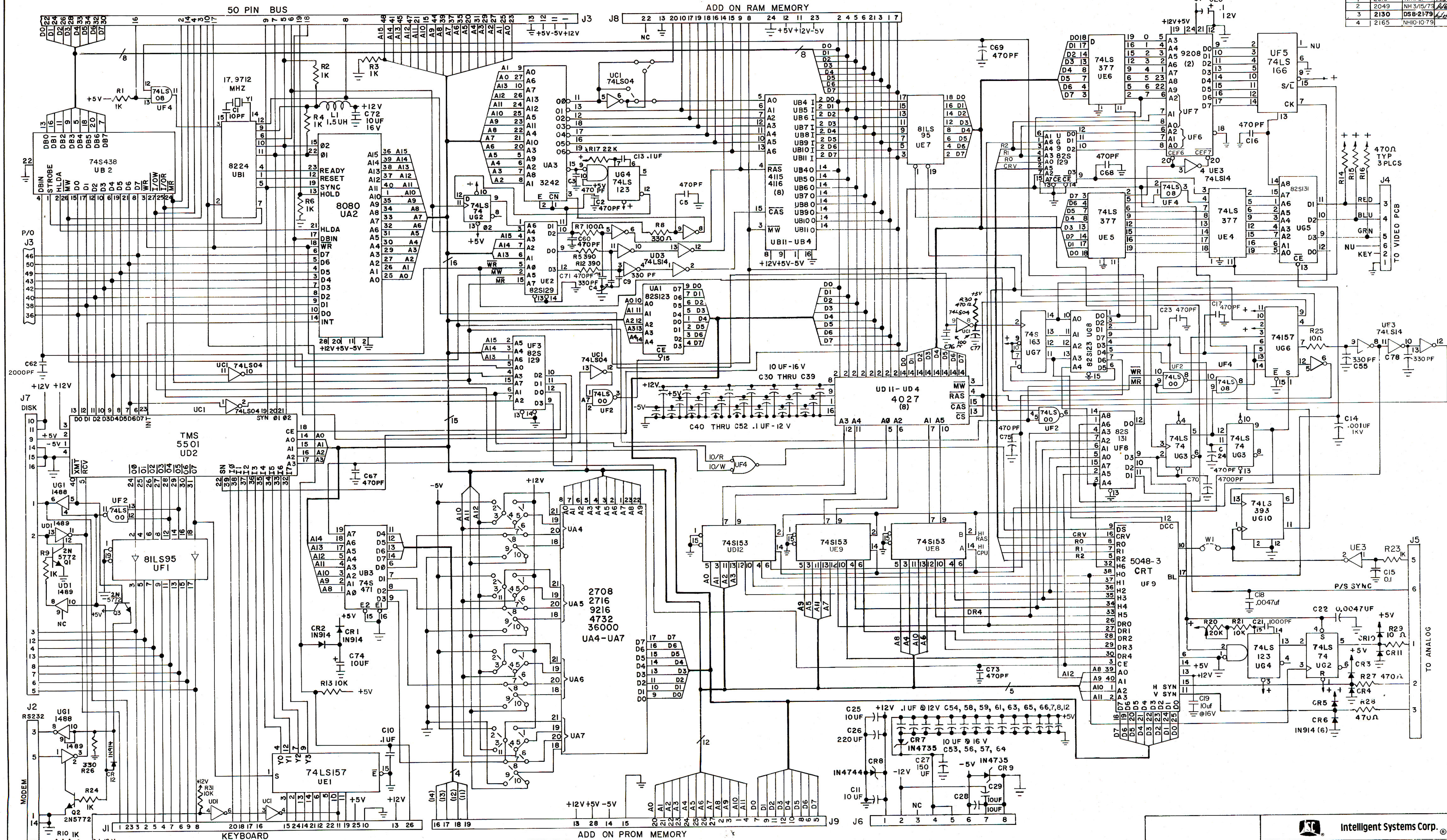
Intelligent Systems Corp.®

© 1978

PN 100962-4

REDUCE TO 10.500 ± .005

REVISIONS			
REV	ECN	DATE	APPROVED
1	2013	NH1/2/79	3/16/79
2	2049	NH3/15/79	3/16/79
3	2130	DS8-21-79	8/29/79
4	2165	NH10-10-79	



INPUT →	+12V	-5V	A12	A10			CS		GND	A11	C5
PATCH NO. →	1	2	3	4	5	6	7	8	9	10	11
ROM IC 2708	X	X					X		X		
ROM IC 2716	X	X				X		X			
ROM IC 4732					X		X			X	X
ROM IC 9216	X			X			X		X		
ROM IC 36000			X		X		X			X	

PATCH 11 IN FOR SOCKETS A5 & A7 ONLY

REF. DESIGNATIONS	
LAST USED	NOT USED
C78	C6,
R32	R18 19 22
CR12	
Q3	
L1	
Y1	
J9	

	DATE
DRAWN N. E. Harris	9-5-78
CHECKED Jim Farris	9-11-78
ENGR: Jim Farris	1-17-79

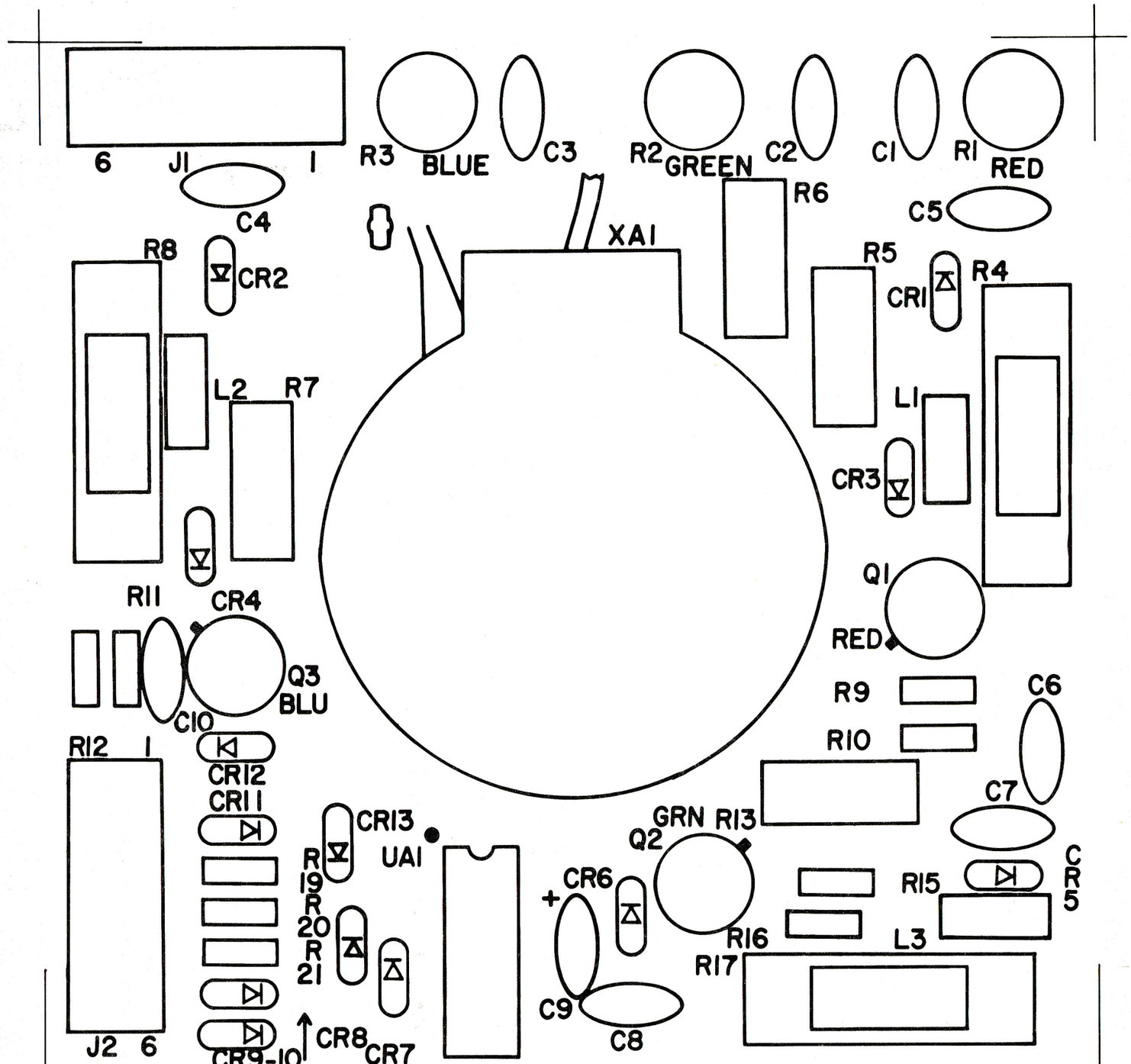
FOR REV 4 PCB

Intelligent Systems Corp.®

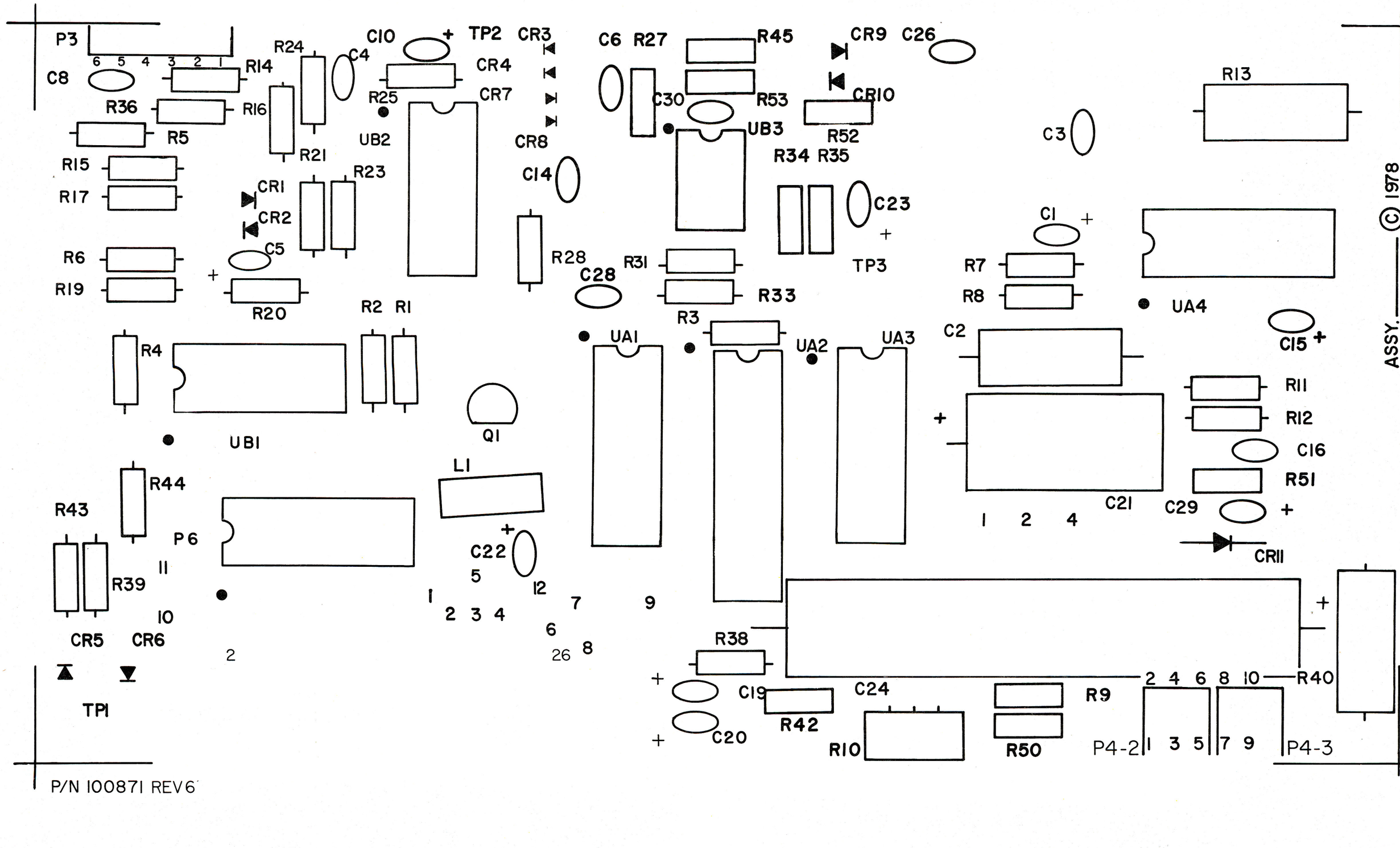
SCHEMATIC LOGIC

SIZE	CODE IDENT NO.	DRAWING NO.	REV.
		100961	4

PN100894-REV6



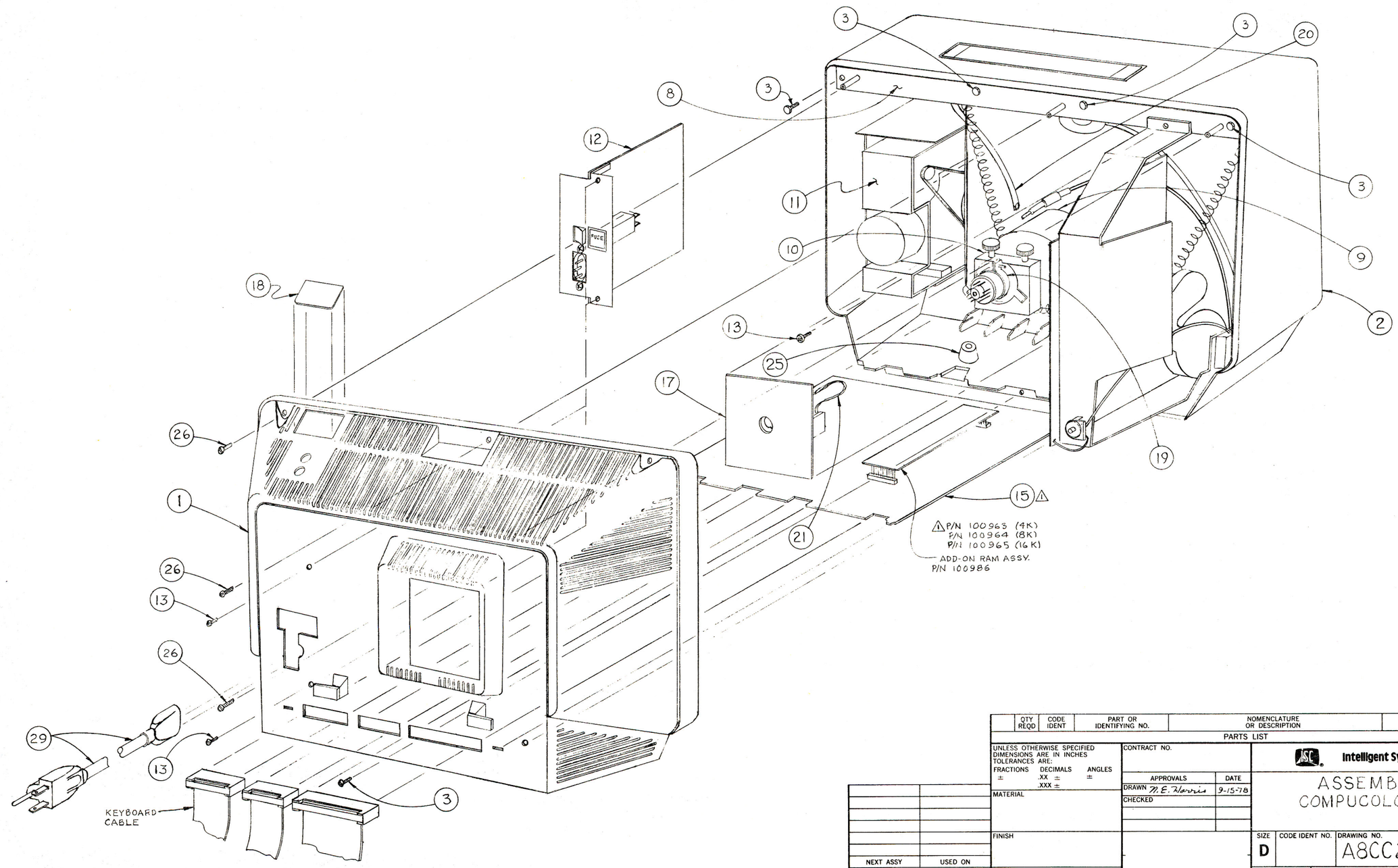
REDUCE TO
4.25±.003



P/N 100871 REV6

ASSY. © 1978

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED



QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION

PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

CONTRACT NO.

APPROVALS	DATE
DRAWN M.E. Harris	9-15-78
CHECKED	

MATERIAL

FINISH

NEXT ASSY | USED ON

APPLICATION

DO NOT SCALE DRAWING

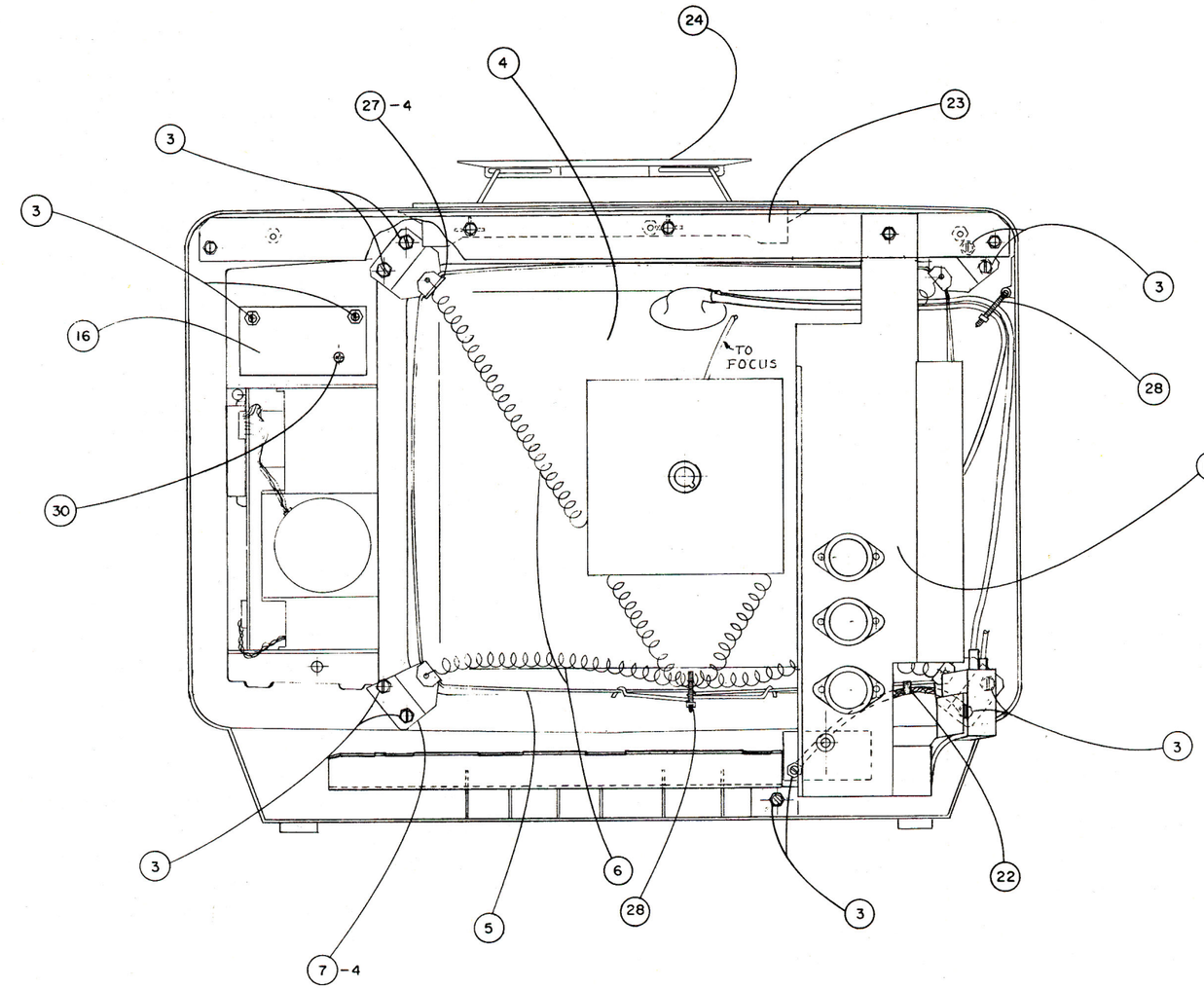
Intelligent Systems Corp. ®

ASSEMBLY COMPUCOLOR II

SIZE	CODE IDENT NO.	DRAWING NO.
D		A8CC23,24,25

SCALE | SHEET 1 OF 3

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED



QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION

PARTS LIST

NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

MATERIAL

FINISH

DO NOT SCALE DRAWING

CONTRACT NO.

APPROVALS	DATE
DRAWN M. E. Harris	9-20-78
CHECKED	

Intelligent Systems Corp.®

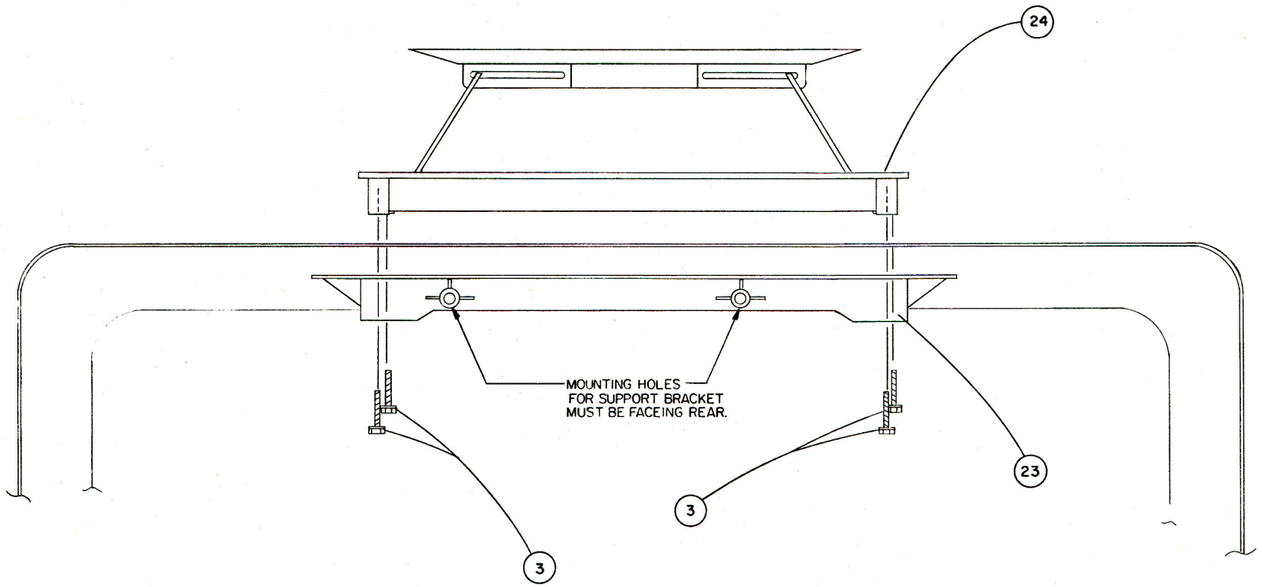
ASSEMBLY, CABINET, FRONT COMPUCOR II

SIZE	CODE IDENT NO.	DRAWING NO.	REV.
D		A8CC23,24,25	

SCALE

SHEET 2 OF 3

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED



QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION

PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

MATERIAL

FINISH

NEXT ASSY | USED ON

APPLICATION

DO NOT SCALE DRAWING

CONTRACT NO.

APPROVALS	DATE
DRAWN I Taylor	6/15/78
CHECKED	

Intelligent Systems Corp.®

ASSEMBLY
HANDLE - COMPUCOLOR II

SIZE	CODE IDENT NO.	DRAWING NO.
D		A8CC23,24,25

SCALE 1/1 | SHEET 3 OF 3

REV	LTR	REVISIONS DESCRIPTION	DATE	APPROVED
4		ADDED IC 74LS138	8-10-78	
5		CHG. C11 (WAS 2000pf) CHG. R19 (WAS 680K) CHG. R25 (WAS 47K) BY N.H. ADD POLARITY TO CAPS.	8-15-78	
6		ADD DIODES CR7 & CR8 BY N.H. CHG. R31 (WAS 100K)	8-29-78	
7		CHANGED: R15 & R16 (WERE 4.7K), R28 & R33 (WERE 10K), R25 (WAS 22K) R10 (WAS 500Ω), C16 (WAS .001μf) REMOVED: R18, R22, R30, R37, C11, C13, C17 ADDED: CR9, CR10, C25 THRU C29, R45 THRU R51	RES 10-12-78	
8		CHG. R16, 17 TO 1K (WERE 2.2K) CHG R19, 17 TO 680K (WERE 1MEG) CHG R20, 29, TO 470Ω (WERE 220Ω) CHG. R28 TO 9.7K (WAS 1K) CHG. R33 TO 8.2K (WAS 3.3K) CHG. R51 TO 100Ω (WAS 330Ω) CHG C8 TO 470 PF (WAS 100PF) CHG. C9 TO 220PF (WAS .001μF) CHG. C29 TO 10μF (WAS 1μF) ADDED IN914. CHG C15 TO 3.3μF (WAS .1μF)	T.T. 11-2-78	
9	A B C D	DELETE R46, 47, 48, 49 DELETE C25, C27 ADDED R52, R53, C30 CHANGED R17 FROM 680K TO 1MEG. CHANGED R19 FROM 680K TO 1MEG. CHANGED R31 FROM 82K TO 120K, CHANGED R33 FROM 8.2K TO 22K, CHANGED R25 FROM 680K TO 22K. (PER ECN # 00212)		
10		CHG R27 (WAS 220Ω) CHG C8 (WAS 470pf) ECN 2006 ECN 2017 ECN 2029 ECN 2042 ECN 2048	1-16-79 1-16-79	AAT 3/16/77
11		CHG R14 FM 4.7K TO 3.3K, CHG R25 FM 33K TO 56K CHG C8 FM 1000PF TO 470 PF ECN 2078	NH 4-27-79	RDN 5/2/79
12		ECN 2110, ECN 2115	7-11-79	RDN 8/1/79

REF DESIGNATIONS	
LAST USED	NOT USED
CR10	
C30	C7, C9, C11, C12, C13, C17, C18, C25, C27
R53	R18, R22, R26, R29, R30, R32, R37, R41
	R46, 47, 48, 49, 36, 50
NEXT ASSY	USED ON
APPLICATION	

QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION

PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

MATERIAL

FINISH

DO NOT SCALE DRAWING

CONTRACT NO.

APPROVALS	DATE
DRAWN Steve Day H. Gow	10-12-77
CHECKED	

Intelligent Systems Corp.

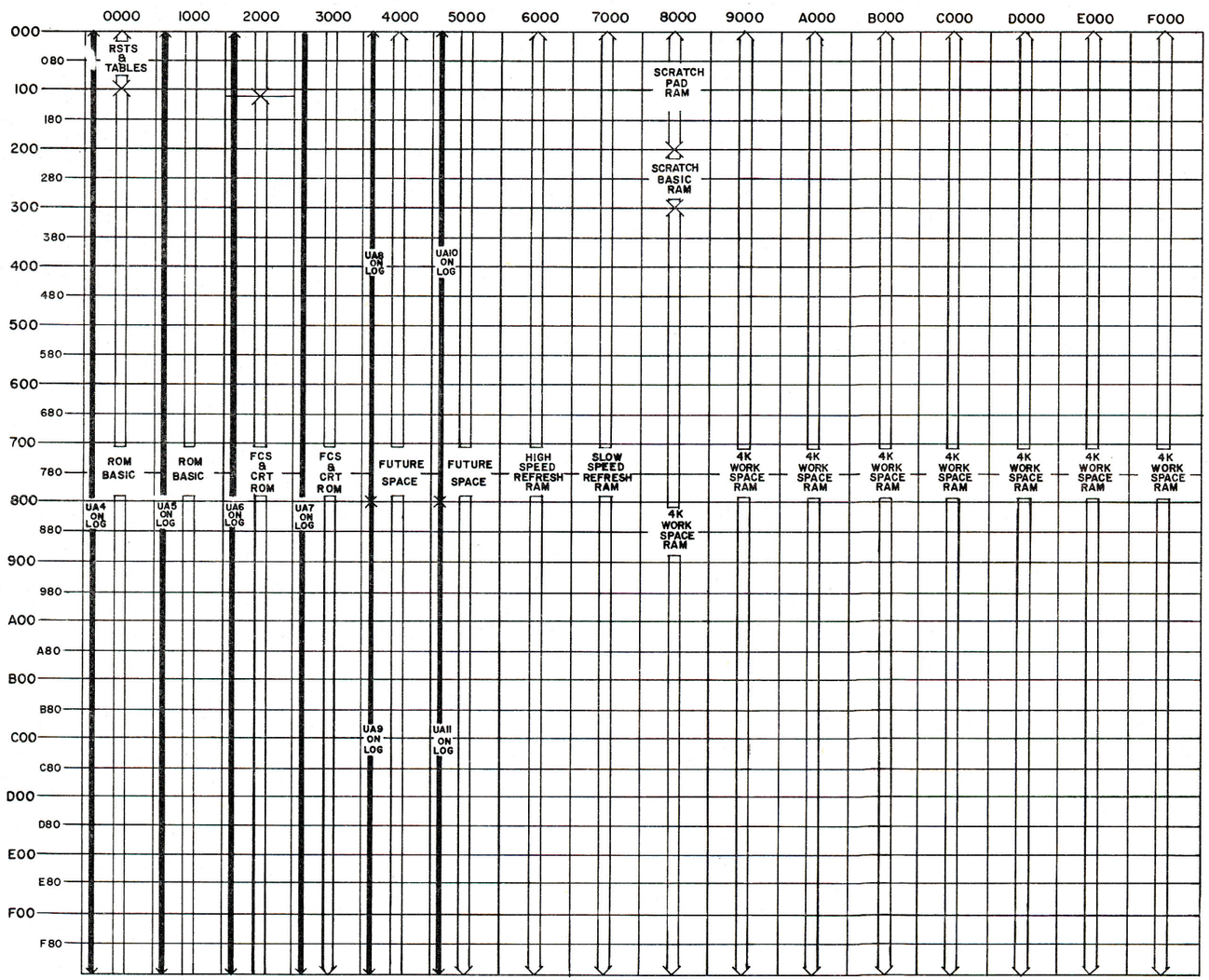
SCHEMATIC
DISK CONTROLLER CC II

SIZE	CODE IDENT NO.	DRAWING NO.	REV.
D		100873	12

SCALE ~ SHEET 1 OF 1

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-9745

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	1	REDRAWN	8-16-78	



QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION

PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

MATERIAL

FINISH

DO NOT SCALE DRAWING

CONTRACT NO.

APPROVALS	DATE
DRAWN T. E. Harris	8-16-78
CHECKED Stanley Hazard	9-11-78

NEXT ASSY | USED ON
APPLICATION

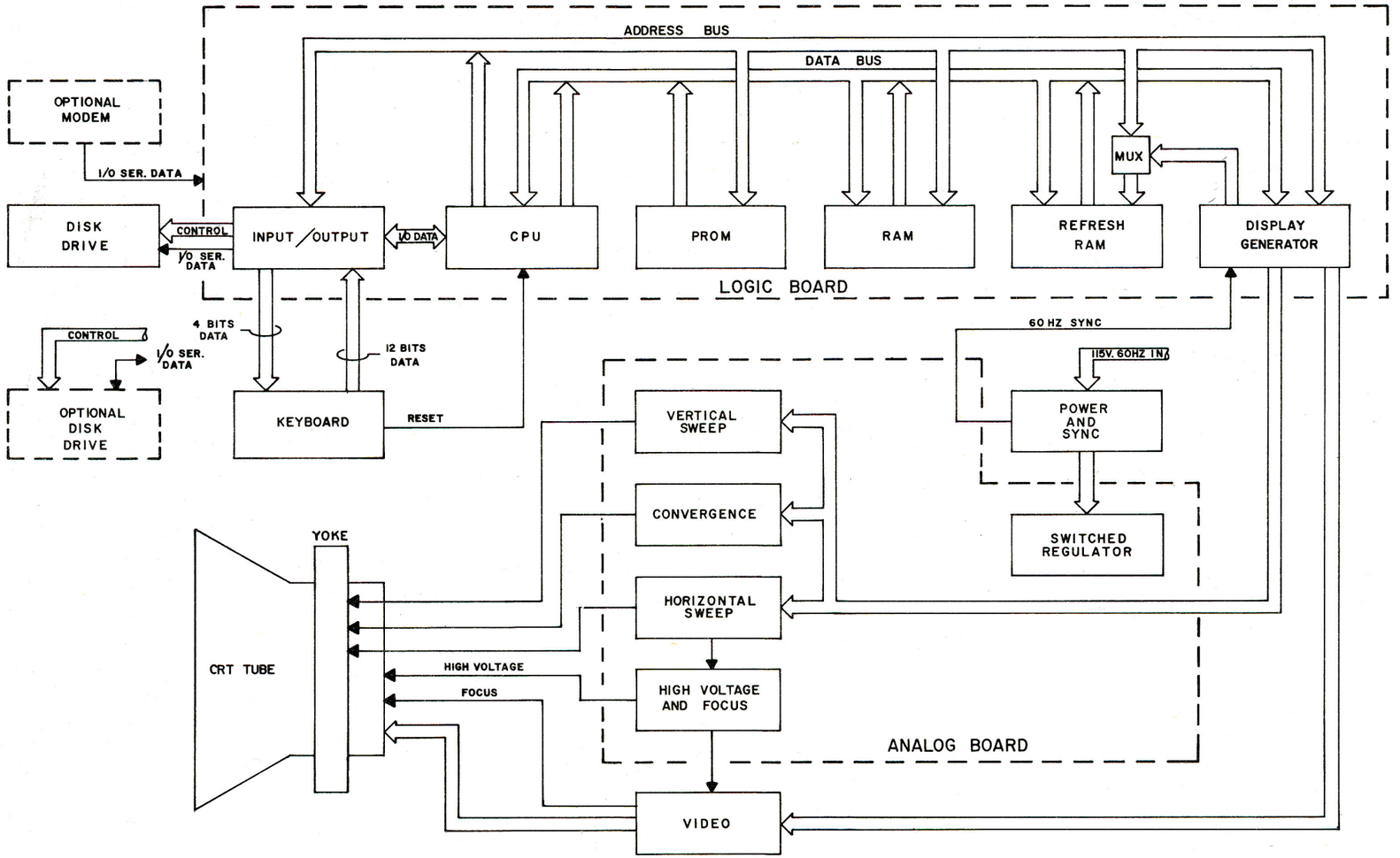
Intelligent Systems Corp.®

MEMORY MAP
COMPUCOLOR II

SIZE	CODE IDENT NO.	DRAWING NO.	REV
D		100991	1

SCALE | SHEET OF

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED



QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION

PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

MATERIAL

FINISH

DO NOT SCALE DRAWING

NEXT ASSY	USED ON
APPLICATION	

CONTRACT NO.

APPROVALS	DATE
DRAWN J.N. Smith	5-2-78
CHECKED Stanley Hazard	9-12-78

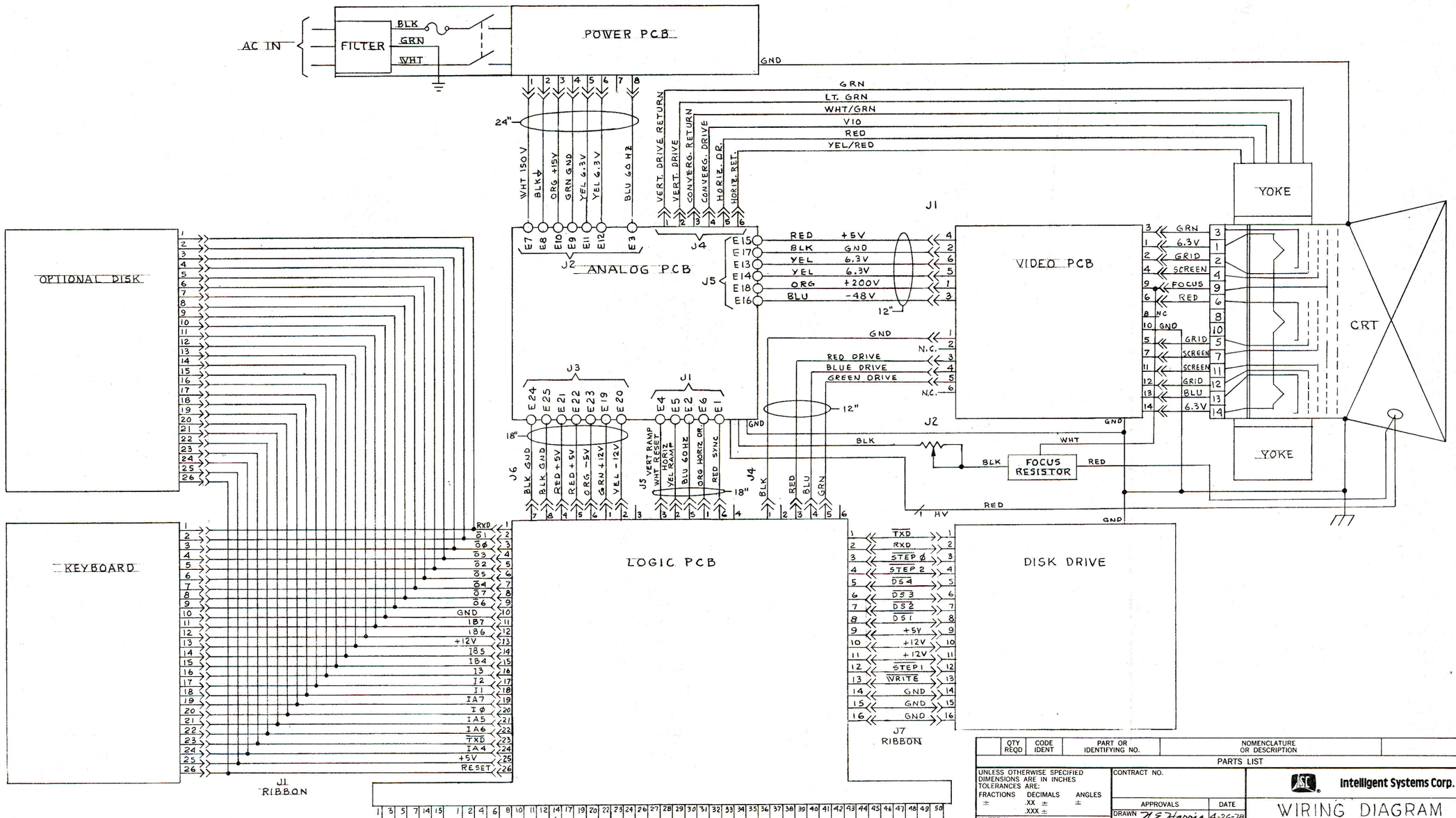
Intelligent Systems Corp.®

COMPUCOLOR II BLOCK DIAGRAM

SIZE	CODE IDENT NO.	DRAWING NO.
D		100995

SCALE —— SHEET 1 OF 1

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED



QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION

PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

MATERIAL

FINISH

NEXT ASSY | USED ON

APPLICATION

DO NOT SCALE DRAWING

CONTRACT NO.

APPROVALS	DATE
DRAWN H. E. Harris	4-26-78
CHECKED John Gayhart	9-12-78

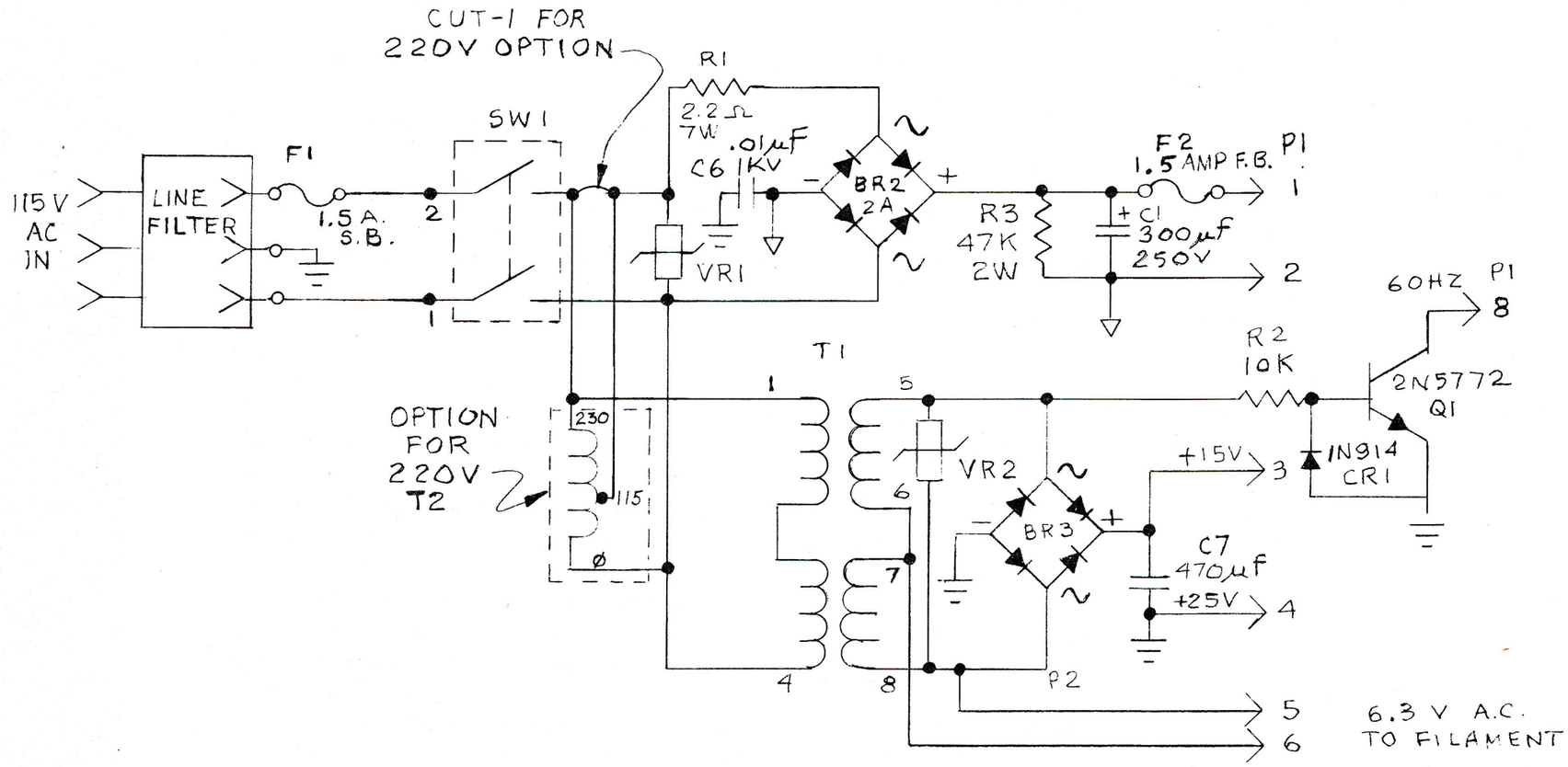
Intelligent Systems Corp.®

WIRING DIAGRAM COMPUCOLOR II

SIZE	CODE IDENT NO.	DRAWING NO.	REV.
D		100990	

SCALE | SHEET OF

REV.	DESCRIPTION	DATE	APPROVED
1	ADD VR1 AHEAD OF SW1 BY N.E.H.	10-12-78	
2	MOVE VR1 AFTER SW1 ADD VR2 SHOW LINE FILTER BY N.E.H.	10-16-78	
3	PROVIDE FOR 220V OPS., ADD T2	12-8-78	



Intelligent Systems Corp.®		
SCALE: ~	APPROVED BY:	DRAWN BY N.E.H.
DATE: 2-8-78		REVISED 10.12.78
SCHEMATIC A/C PWR. SUPPLY C/C II		
		DRAWING NUMBER 100903 3

REVISIONS			
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	1	CHG Q9 (WAS 2N5772) CHG R 69, R89 (WERE 1K) CHG R70, R77, R86 (WERE 10K) CHG R92, R93 (WERE 100Ω) CHG R103 (WAS 20K) CHG R85 (WAS 470K) CHG. C45 (WAS 1μf @35V) CHG C26, C60, C68 C69, C64 & C75 (WERE 3.3μf	8-30-78	
	2	CHG R17 FROM 10Ω 2W TO 2, 4.7Ω 2W IN SERIES	11-1-78	
	3	ADDED TWO 1200μf 8.15V CAPS IN SERIES WITH R70 AND R106	11-2-78	

SEPARATE POWER P.C.B.

HORIZ RAMP

HORIZ. RAMP RESET

VERT. RAMP

VERTICAL RAMP RESET

PINCUSHION WAVEFORM

VERT HEIGHT

RIGHT

LEFT

BOTTOM

TOP

FOCUS POT.

FOCUS NOT ON BOARD

25K ANODE

6.3 V AC TO FILAMENT

AC POWER BOARD

VIDEO BOARD

DIGITAL

HORIZ.

FBT 1

QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION

PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

MATERIAL

FINISH

DO NOT SCALE DRAWING

NEXT ASSY	USED ON
APPLICATION	

CONTRACT NO.

APPROVALS	DATE
DRAWN M. E. Harris	2-8-77
CHECKED Stanley Hazel	9-12-78

Intelligent Systems Corp.

SCHEMATIC
ANALOG CC II

SIZE	CODE IDENT NO.	DRAWING NO.	REV
D		100902	3

SCALE | SHEET 1 OF 1

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-9745

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
		RELIESED	12-18-78	

PRELIMINARY

PRELIMINARY

QTY REQD	CODE IDENT	PART OR IDENTIFYING NO	NOMENCLATURE OR DESCRIPTION

PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE
FRACTIONS DECIMALS ANGLES
XX
XXX

CONTRACT NO

APPROVALS	DATE
DRAWN M. E. Harris	2-8-78
CHECKED S. Hagan	2-9-78

MATERIAL

FINISH

NEXT ASSY | USED ON

APPLICATION

DO NOT SCALE DRAWING

Intelligent Systems Corp.®

SCHEMATIC ANALOG CC II

SIZE	CODE IDENT NO	DRAWING NO	REV.
D		100902	4

SCALE | SHEET 1 OF 1

APPENDIX A
TMS 8080 MICROPROCESSOR

TMS 8080 Microprocessor

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

TMS 8080 MICROPROCESSOR

1. ARCHITECTURE

1.1 INTRODUCTION

The TMS 8080 is an 8-bit parallel central processing unit (CPU) fabricated on a single chip using a high-speed N-channel silicon-gate process. (See Figure 1). A complete microcomputer system with a 2-μs instruction cycle can be formed by interfacing this circuit with any appropriate memory. Separate 8-bit data and 16-bit address buses simplify the interface and allow direct addressing of 65,536 bytes of memory. Up to 256 input and 256 output ports are also provided with direct addressing. Control signals are brought directly out of the processor and all signals, excluding clocks, are TTL compatible.

1.2 THE STACK

The TMS 8080 incorporates a stack architecture in which a portion of external memory is used as a pushdown stack for storing data from working registers and internal machine status. A 16-bit stack pointer (SP) is provided to facilitate stack location in the memory and to allow almost unlimited interrupt handling capability. The CALL and RST (restart) instructions use the SP to store the program counter (PC) into the stack. The RET (return) instruction uses the SP to acquire the previous PC value. Additional instructions allow data from registers and flags to be saved in the stack.

1.3 REGISTERS

The TMS 8080 has three categories of registers: general registers, program control registers, and internal registers. The general registers and program control registers are listed in Table 1. The internal registers are not accessible by the programmer. They include the instruction register, which holds the present instruction, and several temporary storage registers to hold internal data or latch input and output addresses and data.

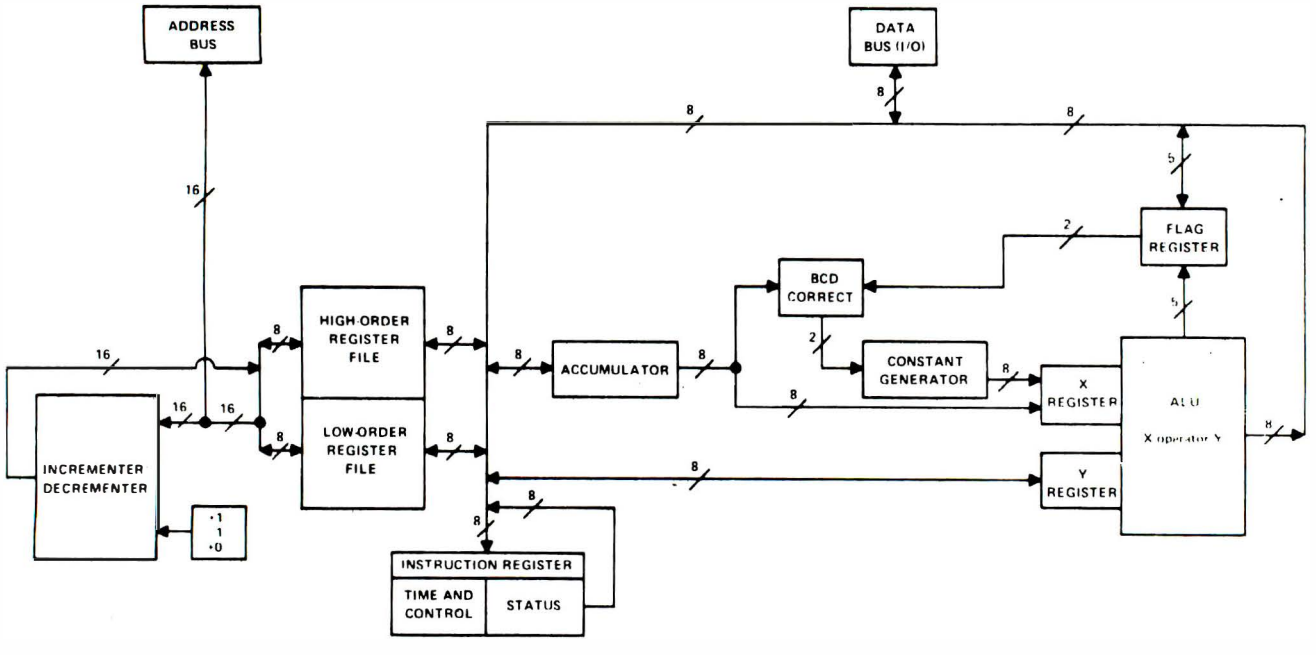


FIGURE 1–TMS 8080 FUNCTIONAL BLOCK DIAGRAM

1.4 THE ARITHMETIC UNIT

Arithmetic operations are performed in an 8-bit parallel arithmetic unit that has both binary and decimal capabilities. Four testable internal flag bits are provided to facilitate program control, and a fifth flag is used for decimal corrections. Table 2 defines these flags and their operation. Decimal corrections are performed with the DAA instruction. The DAA corrects the result of binary arithmetic operation on BCD data as shown in Table 3.

1.5 STATUS AND CONTROL

Two types of status are provided by the TMS8080. Certain status is indicated by dedicated control lines. Additional status is transmitted on the data bus during the beginning of each instruction cycle (machine cycle). Table 4 indicates the pin functions of the TMS8080. Table 5 defines the status information that is presented during the beginning of each machine cycle (SYNC time) on the data bus.

1.6 I/O OPERATIONS

Input/output operations (I/O) are performed using the IN and OUT instructions. The second byte of these instructions indicates the device address (256 device addresses). When an IN instruction is executed, the input device address appears in duplicate on A7 through A0 and A15 through A8, along with $\overline{WO}$ and INP status on the data bus. The addressed input device then puts its input data on the data bus for entry into the accumulator. When an OUT instruction is executed, the same operation occurs except that the data bus has OUT status and then has output data.

Direct memory access channels (DMA) can be OR-tied directly with the data and address buses through the use of the HOLD and HLDA (hold acknowledge) controls. When a HOLD request is accepted by the CPU, HLDA goes high, the address and data lines are forced to a high-impedance or "floating" condition, and the CPU stops until the HOLD request is removed.

Interfacing with different speed memories is easily accomplished by use of the WAIT and READY pins. During each machine cycle, the CPU polls the READY input and enters a wait condition until the READY line becomes true. When the WAIT output pin is high, it indicates that the CPU has entered the wait state.

Designing interrupt driven systems is simplified through the use of vectored interrupts. At the end of each instruction, the CPU polls the INT input to determine if an interrupt request is being made. This action does not occur if the CPU is in the HOLD state or if interrupts are disabled. The INTE output indicates if the interrupt logic is enabled (INTE is high). When a request is honored, the INTA status bit becomes high, and an RST instruction may be inserted to force the CPU to jump to one of eight possible locations. Enabling or disabling interrupts is controlled by special instructions (EI or DI). The interrupt input is automatically disabled when an interrupt request is accepted or when a RESET signal is received.

1.7 INSTRUCTION TIMING

The execution time of the instructions varies depending on the operation required and the number of memory references needed. A machine cycle is defined to be a memory referencing operation and is either 3, 4, or 5 state times long. A state time (designated S) is a full cycle of clocks $\phi 1$ and $\phi 2$. (NOTE: The exception to this rule is the DAD instruction, which consists of 1 memory reference in 10 state times). The first machine cycle (designated M1) is either 4 or 5 state times long and is the "instruction fetch" cycle with the program counter appearing on the address bus. The CPU then continues with as many M cycles as necessary to complete the execution of the instruction (up to a maximum of 5). Thus the instruction execution time varies from 4 state times (several including ADDr) to 18 (XTHL). The WAIT or HOLD conditions may affect the execution time since they can be used to control the machine (for example to "single step") and the HALT instruction forces the CPU to stop until an interrupt is received. As the instruction execution is completed (or in the HALT state) the INT pin is polled for an interrupt. In the event of an interrupt, the PC will not be incremented during the next M1 and an RST instruction can be inserted.

TABLE 1
TMS 8080 REGISTERS

NAME	DESIGNATOR	LENGTH	PURPOSE
Accumulator	A	8	Used for arithmetic, logical, and I/O operations
B Register	B	8	General or most significant 8 bits of double register BC
C Register	C	8	General or least significant 8 bits of double register BC
D Register	D	8	General or most significant 8 bits of double register DE
E Register	E	8	General or least significant 8 bits of double register DE
H Register	H	8	General or most significant 8 bits of double register HL
L Register	L	8	General or least significant 8 bits of double register HL
Program Counter	PC	16	Contains address of next byte to be fetched
Stack Pointer	SP	16	Contains address of the last byte of data saved in the memory stack
Flag Register	F	5	Five flags (C, Z, S, P, C1)

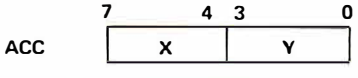
NOTE: Registers B and C may be used together as a single 16 bit register, likewise, D and E, and H and L.

TABLE 2

FLAG DESCRIPTIONS

SYMBOL	TESTABLE	DESCRIPTION
C	YES	C is the carry/borrow out of the MSB (most significant bit) of the ALU (Arithment Logic Unit). A TRUE condition (C = 1) indicates overflow for addition or underflow for subtraction.
Z	YES	A TRUE condition (Z = 1) indicates that the output of the ALU is equal to zero.
S	YES	A TRUE condition (S = 1) indicates that the MSB of the ALU output is equal to a one (1).
P	YES	A TRUE condition (P = 1) indicates that the output of the ALU has even parity (the number of bits equal to one is even).
C1	NO	C1 is the carry out of the fourth bit of the ALU (TRUE condition). C1 is used only for BCD correction with the DAA instruction.

TABLE 3
FUNCTION OF THE DAA INSTRUCTION
Assume the accumulator (A) contains two BCD digits, X and Y



ACCUMULATOR BEFORE DAA				ACCUMULATOR AFTER DAA			
C	$A_7 \ldots A_4$	C1	$A_3 \ldots A_0$	C	$A_7 \ldots A_4$	C1	$A_3 \ldots A_0$
0	X < 10	0	Y < 10	0	X	0	Y
0	X < 10	1	Y < 10	0	X	0	Y + 6
0	X < 9	0	Y ≥ 10	0	X + 1	1	Y + 6
1	X < 10	0	Y < 10	1	X + 6	0	Y
1	X < 10	1	Y < 10	1	X + 6	0	Y + 6
1	X < 10	0	Y ≥ 10	1	X + 7	1	Y + 6
0	X ≥ 10	0	Y < 10	1	X + 6	0	Y
0	X ≥ 10	1	Y < 10	1	X + 6	0	Y + 6
0	X ≥ 9	0	Y ≥ 10	1	X + 7	1	Y + 6

NOTE: The corrections shown in Table 3 are sufficient for addition. For subtraction, the programmer must account for the borrow condition that can occur and give erroneous results. The most straight forward method is to set A = 99_{16} and carry = 1. Then add the minuend to A after subtracting the subtrahend from A.

TABLE 4
TMS 8080 PIN DEFINITIONS

SIGNATURE	PIN	I/O	DESCRIPTION
A15 (MSB)	36	OUT	A15 through A0 comprise the address bus. True memory or I/O device addresses appear on this 3-state bus during the first state time of each instruction cycle.
A14	39	OUT	
A13	38	OUT	
A12	37	OUT	
A11	40	OUT	
A10	1	OUT	
A9	35	OUT	
A8	34	OUT	
A7	33	OUT	
A6	32	OUT	
A5	31	OUT	
A4	30	OUT	
A3	29	OUT	
A2	27	OUT	
A1	26	OUT	
A0 (LSB)	25	OUT	
D7 (MSB)	6	IN/OUT	D7 through D0 comprise the bidirectional 3-state data bus. Memory, status, or I/O data is transferred on this bus.
D6	5	IN/OUT	
D5	4	IN/OUT	
D4	3	IN/OUT	
D3	7	IN/OUT	
D2	8	IN/OUT	
D1	9	IN/OUT	
D0 (LSB)	10	IN/OUT	
V_{SS}	2		Ground reference
V_{BB}	11		Supply voltage (−5 V nominal)
V_{CC}	20		Supply voltage (5 V nominal)
V_{DD}	28		Supply voltage (12 V nominal)
$\phi 1$	22	IN	Phase 1 clock.
$\phi 2$	15	IN	Phase 2 clock. See page 19 for $\phi 1$ and $\phi 2$ timing.
RESET	12	IN	Reset. When active (high) for a minimum of 3 clock cycles, the RESET input causes the TMS 8080 to be reset. PC is cleared, interrupts are disabled, and after RESET, instruction execution starts at memory location 0. To prevent a lockup condition, a HALT instruction must not be used in location 0.
HOLD	13	IN	Hold signal. When active (high) HOLD causes the TMS 8080 to enter a hold state and float (put the 3-state address and data bus in a high-impedance state). The chip acknowledges entering the hold state with the HLDA signal and will not accept interrupts until it leaves the hold state.
INT	14	IN	Interrupt request. When active (high) INT indicates to the TMS8080 that an interrupt is being requested. The TMS8080 polls INT during a HALT or at the end of an instruction. The request will be accepted except when INTE is low or the CPU is in the HOLD condition.
INTE	16	OUT	Interrupts enabled. INTE indicates that an interrupt will be accepted by the TMS 8080 unless it is in the hold state. INTE is set to a high logic level by the EI (Enable Interrupt) instruction and reset to a low logic level by the DI (Disable Interrupt) instruction. INTE is also reset when an interrupt is accepted and by a high on RESET.
DBIN	17	OUT	Data bus in. DBIN indicates whether the data bus is in an input or an output mode. (high = input, low = output).

TABLE 4 (CONTINUED)

SIGNATURE	PIN	I/O	DESCRIPTION
$\overline{WR}$	18	OUT	Write. When active (low) $\overline{WR}$ indicates a write operation on the data bus to memory or to an I/O port.
SYNC	19	OUT	Synchronizing control line. When active (high) SYNC indicates the beginning of each machine cycle of the TMS8080. Status information is also present on the data bus during SYNC for external latches.
HLDA	21	OUT	Hold acknowledge. When active (high) HLDA indicates that the TMS8080 is in a hold state.
READY	23	IN	Ready control line. An active (high) level indicates to the TMS 8080 that an external device has completed the transfer of data to or from the data bus. READY is used in conjunction with WAIT for different memory speeds.
WAIT	24	OUT	Wait status. When active (high) WAIT indicates that the TMS8080 has entered a wait state pending a READY signal from memory.

TABLE 5

TMS 8080 STATUS

SIGNATURE	DATA BUS BIT	DESCRIPTION
INTA	D0	Interrupt acknowledge.
$\overline{WO}$	D1	Indicates that current machine cycle will be a read (input) (high = read) or a write (output) (low = write) operation.
STACK	D2	Indicates that address is stack address from the SP.
HLTA	D3	HALT instruction acknowledge.
OUT	D4	Indicates that the address bus has an output device address and the data bus has output data.
M1	D5	Indicates instruction acquisition for first byte.
INP	D6	Indicates address bus has address of input device.
MEMR	D7	Indicates that data bus will be used for memory read data.

2. TMS 8080 INSTRUCTION SET

2.1 INSTRUCTION FORMATS

TMS 8080 instructions are either one, two, or three bytes long and are stored as binary integers in successive memory locations in the format shown below.

One-Byte Instructions

D7 D6 D5 D4 D3 D2 D1 D0	OP CODE

Two-Byte Instructions

D7 D6 D5 D4 D3 D2 D1 D0	OP CODE
D7 D8 D5 D4 D3 D2 D1 D0	OPERAND

Three-Byte Instructions

D7 D6 D5 D4 D3 D2 D1 D0	OP CODE
D7 D6 D5 D4 D3 D2 D1 D0	LOW ADDRESS OR OPERAND 1
D7 D6 D5 D4 D3 D2 D1 D0	HIGH ADDRESS OR OPERAND 2

2.2 INSTRUCTION SET DESCRIPTION

Operations resulting from the execution of TMS 8080 instructions are described in this section. The flags that are affected by each instruction are given after the description.

2.2.1 INSTRUCTION SYMBOLS

SYMBOL	DESCRIPTION
<b_2>	Second byte of instruction
<b_3>	Third byte of instruction
r_a	Register # = 000 → B; 001 → C; 010 → D; 011 → E; 100 → H; 101 → L; 111 → A
r_b	Register # = 00 → BC; 01 → DE; 10 → HL; 11 → SP
r_c	Register # = 0 → BC; 1 → DE
r_d	Register # = 00 → BC; 01 → DE; 10 → HL
r_dL	Least significant 8 bits of r_d
r_dH	Most significant 8 bits of r_d
f	Flags: Zero (Z) — Result is zero; Carry (C) — Carry/borrow out of MSB is one; Parity (P) — Parity of result is even; Sign (S) — MSB of result is one; Carry 1 (C1) — Carry out of fourth bit is one
M	Memory address defined by registers H and L
( )	Contents of specified address or register
[ ]	Contents at address contained in specified register
←	Is transferred to
↔	Exchange
Am	Bit m of A register (accumulator)
⦀	Flags affected
b_2	Single byte immediate operand
b_3b_2	Double byte immediate operand
$(nnn)_8$	(nnn) is an octal (base 8) number

2.2.2 ACCUMULATOR GROUP INSTRUCTIONS

MNEMONIC	OPERANDS	BYTES	M CYCLES/ STATES	DESCRIPTION
ACI	b_2	2	2/7	(A) ← (A) + <b_2>+(carry), add the second byte of the instruction and the contents of the carry flag to register A and place in A. {C,Z,S,P,C1}
ADC	M	1	2/7	(A) ← (A) + (M) + (carry). {C,Z,S,P,C1}
ADC	r_a	1	1/4	(A) ← (A) + (r_a) + (carry). {C,Z,S,P,C1}
ADD	M	1	2/7	(A) ← (A) + (M), add the contents of M to register A and place in A. {C,Z,S,P,C1}
ADD	r_a	1	1/4	(A) ← (A) + (r_a).{C,Z,S,P,C1}
ADI	b_2	2	2/7	(A) ← (A) + <b_2>. {C,Z,S,P,C1}
ANA	M	1	2/7	(A) ← (A) AND (M), take the logical AND of M and register A and place in A. The carry flag will be reset low. {C,Z,S,P,C1}
ANA	r_a	1	1/4	(A) ← (A) AND (r_a). {C,Z,S,P,C1}
ANI	b_2	2	2/7	(A) ← (A) AND <b_2>. {C,Z,S,P,C1}
CMA		1	1/4	(A) ← ($\bar{A}$), complement A.
CMC		1	1/4	(carry) ← ($\overline{carry}$), complement the carry flag. {C}
CMP	M	1	2/7	(A) – (M), compare the contents of M to register A and set the flags accordingly. {C,Z,S,P,C1} (A) = (M) Z = 1 (A) ≠ (M) Z = 0 (A) < (M) C = 1 (A) > (M) C = 0
CMP	r_a	1	1/4	(A) – (r_a). {C,Z,S,P,C1}
CPI	b_2	2	2/7	(A)–<b_2>. {C,Z,S,P,C1}
DAA		1	1/4	(A)←BCD correction of (A). The 8 bit A contents is corrected to form two 4 bit BCD digits after a binary arithmetic operation. A fifth flag C1 indicates the overflow from A_3. The carry flag C indicates the overflow from A_7 (See Table 3). {C,Z,S,P,C1}
DAD	r_b	1	1/10	(HL) ← (HL) + (r_b), add the contents of double register r_b to double register HL and place in HL. {C}
LDA	b_3b_2	3	4/13	(A)←[<b_3> <b_2>]
LDAX	r_c	1	2/7	(A)←[(r_c)]
ORA	M	1	2/7	(A) ← (A) OR (M), take the logical OR of the contents of M and register A and place in A. The carry flag will be reset. {C,Z,S,P,C1}
ORA	r_a	1	1/4	(A) ← (A) OR (r_a).{C,Z,S,P,C1}
ORI	b_2	2	2/7	(A) ← (A) OR <b_2>. {C,Z,S,P,C1}
RAL		1	1/4	A_{m+1}←A_m, A_0←(carry), (carry)←(A_7). Shift the contents of register A to the left one bit through the carry flag. {C}
RAR		1	1/4	A_m←A_{m+1}, A_7←(carry), (carry)←A_0. {C}
RLC		1	1/4	A_{m+1}←A_m, A_0←A_7 (carry)←(A_7). Shift the contents of register A to the left one bit. Shift A_7 into A and into the carry flag. {C}
RRC		1	1/4	A_m←A_{m+1}, A_7←A_0, (carry)←(A_0). {C}

MNEMONIC	OPERANDS	BYTES	M CYCLES/ STATES	DESCRIPTION
SBB	M	1	2/7	(A)←(A)−(M)−(carry), subtract the contents of M and the contents of the carry flag from register A and place in A. Two's complement subtraction is used and a true borrow causes the carry flag to be set (underflow condition). {C,Z,S,P,C1}
SBB	r_a	1	1/4	(A)←(A)−(r_a)−(carry). {C,Z,S,P,C1}
SBI	b_2	2	2/7	(A)←(A)−<b_2>−(carry). {C,Z,S,P,C1}
STA	b_3b_2	3	4/13	[<b_3> <b_2>]←(A), store contents of A in memory address given in bytes 2 and 3.
STAX	r_c	1	2/7	[(r_c)]←(A), store contents of A in memory address given in BC or DE.
STC		1	1/4	(carry)←1, set carry flag to a 1 (true condition).
SUB	M	1	2/7	(A)←(A)−(M), subtract the contents of M from register A and place in A. Two's complement subtraction is used and a true borrow causes the carry flag to be set (underflow condition). {C,Z,S,P,C1}
SUB	r_a	1	1/4	(A)←(A)−(r_a).{C,Z,S,P,C1}
SUI	b_2	2	2/7	(A)←(A)−<b_2>. {C,Z,S,P,C1}
XRA	M	1	2/7	(A)←(A) XOR (M), take the exclusive OR of the contents of M and register A and place in A. The carry flag will be reset. {C,Z,S,P,C1}
XRA	r_a	1	1/4	(A)←(A) XOR (r_a). {C,Z,S,P,C1}
XRI	b_2	2	2/7	(A)←(A) XOR <b_2>. {C,Z,S,P,C1}

2.2.3 INPUT/OUTPUT INSTRUCTIONS

MNEMONIC	OPERANDS	BYTES	M CYCLES/ STATES	DESCRIPTION
IN	b_2	2	3/10	(A)←(input data from data bus), byte 2 is sent on bits A7-A0 and A15-A8 as the input device address. INP status is given on the data bus.
OUT	b_2	2	3/10	(Output data)←(A), byte 2 is sent on bits A7-A0 and A15-A8 as the output device address. OUT status is given on the data bus.

2.2.4 MACHINE INSTRUCTIONS

MNEMONIC	OPERANDS	BYTES	M CYCLES/ STATES	DESCRIPTION
HLT		1	2/7	Halt, all machine operations stop. All registers are maintained. Only an interrupt can return the TMS 8080 to the run mode. Note that a HLT should not be placed in location zero, otherwise after the reset pin is active, the TMS 8080 will enter a nonrecoverable state (until power is removed), i.e., in halt with interrupts disabled. This condition also occurs if a HLT is executed while interrupts are disabled. HLTA status is given on the data bus.
NOP		1	1/4	(PC)←(PC)+1, no operation.

2.2.5 PROGRAM COUNTER AND STACK CONTROL INSTRUCTIONS

MNEMONIC	OPERANDS	BYTES	M CYCLES/ STATES	DESCRIPTION
CALL	b_3b_2	3	5/17	[(SP)−1] [(SP)−2]←(PC), (SP)←(SP)−2, (PC)←<b_3> <b_2>, transfer PC to the stack address given by SP, decrement SP twice, and jump unconditionally to address given in bytes 2 and 3.
Conditional call instructions for true flags:				
(f)			5/17 (Pass)	If (f) = 1, [(SP)−1] [(SP)−2]←(PC), (SP)←(SP)−2, (PS)←<b_3> <b_2>, otherwise (PC)←(PC)+3. If the flag specified, f, is 1, then execute a call. Otherwise, execute the next instruction.
CC (carry)	b_3b_2	3	3/11 (Fail)	
CPE (parity)	b_3b_2	3		
CM (sign)	b_3b_2	3		
CZ (zero)	b_3b_2	3		
Conditional call instructions for false flags:				
(f)			5/17 (Pass)	If (f) = 0, [(SP)−1] [(SP)−2]←(PC), (SP)←(SP)−2, (PC)←<b_3> <b_2>, otherwise (PC)←(PC)+3.
CNC (carry)	b_3b_2	3	3/11 (Fail)	
CPO (parity)	b_3b_2	3		
CP (sign)	b_3b_2	3		
CNZ (zero)	b_3b_2	3		
DI		1	1/4	Disable interrupts. INTE is driven false to indicate that no interrupts will be accepted.
EI		1	1/4	Enable interrupts. INTE is driven true to indicate that an interrupt will be accepted. Execution of this instruction is delayed to allow the next instruction to be executed before the INT input is polled.
JMP	b_3b_2	3	3/10	(PC)←<b_3> <b_2>, jump unconditionally to address given in bytes 2 and 3.
Conditional jump instructions for true flags:				
(f)			3/10	If (f) = 1, (PC)←<b_3><b_2>, otherwise (PC)←(PC)+3. If the flag specified, f, is 1, execute a JMP. Otherwise, execute the next instruction.
JC (carry)	b_3b_2	3		
JPE (parity)	b_3b_2	3		
JM (sign)	b_3b_2	3		
JZ (zero)	b_3b_2	3		
Conditional jump instructions for false flags:				
(f)			3/10	If (f) = 0, (PC)←<b_3> <b_2>, othewise (PC)←(PC)+3.
JNC (carry)	b_3b_2	3		
JPO (parity)	b_3b_2	3		
JM (sign)	b_3b_2	3		
JNZ (zero)	b_3b_2	3		
PCHL		1	1/5	(PC)←(HL)
POP	PSW	1	3/10	(F)←[(SP)], (A)←[(SP)+1], (SP)←(SP)+2, restore the last stack values addressed by SP into A and F. Increment SP twice.
POP	r_d	1	3/10	(r_{dL})←[(SP)], (r_{dH})←[(SP)+1], (SP)←(SP)+2.
PUSH	PSW	1	3/11	[(SP)−1]←(A), [(SP)−2]←(F), (SP)←(SP)−2, save the contents of A and F into the stack addressed by SP. Decrement SP twice.
PUSH	r_d	1	3/11	[(SP)−1]←(r_{dL}), [(SP)−2]←(r_{dH}), (SP)←(SP)−2.
RET		1	3/10	(PC)←[(SP)] [(SP)+1], (SP)←(SP)+2, return to program at memory address given by last values in the stack. The SP is incremented by two.

MNEMONIC	OPERANDS	BYTES	M CYCLES/ STATES	DESCRIPTION
Conditional return instructions for true flags:				
	(f)		3/11 (Pass)	If (f) = 1, (PC)←[(SP)] [(SP+1], (SP)←(SP)+2. If the flag specified, f, is 1, execute a RET. Otherwise, execute the next instruction.
RC	(carry) C	1	1/5 (Fail)	
RPE	(parity) P	1		
RM	(sign) S	1		
RZ	(zero) Z	1		
Conditional return instructions for false flags:				
	(f)		3/11 (Pass)	If (f) = 0, (PC)←[(SP)] [(SP)+1], (SP)←(SP)+2.
RNC	(carry) C	1	1/5 (Fail)	
RPO	(parity) P	1		
RP	(sign) S	1		
RNZ	(zero) Z	1		
RST		1	3/11	[(SP)−1] [(SP)−2] ← (PC) (SP)← (SP)−2, (PC)←0000R0$_8$ where R is a 3 bit field in RST (RST=3R7$_8$). Transfer PC to the stack address given by SP, decrement SP twice, and jump to the address specified by R.
SPHL		1	1/5	(SP)←(HL).

2.2.6 REGISTER GROUP INSTRUCTIONS

MNEMONIC	OPERANDS	BYTES	M CYCLES/ STATES	DESCRIPTION
DCR	M	1	3/10	(M)←(M)−1, decrement the contents of memory location specified by H and L. {Z,S,P,C1}
DCR	r_a	1	1/5	(r_a)←(r_a)−1, decrement the contents of register r_a. {Z,S,P,C1}
DCX	r_b	1	1/5	(r_b)←(r_b)−1, decrement double registers BC, DE, HL, or SP.
INR	M	1	3/10	(M)←(M)+1, increment the contents of memory location specified by H and L. {Z,S,P,C1}
INR	r_a	1	1/5	(r_a)←(r_a)+1, increment the contents of register r_a. {Z,S,P,C1}
INX	r_b	1	1/5	(r_b)←(r_b)+1, increment double registers BC, DE, HL, or SP.
LHLD	b_3b_2	3	5/16	(L)←[<b_3> <b_2>]; (H)← [<b_3> <b_2>+1], load registers H and L with contents of the two memory locations specified by bytes 3 and 2.
LXI	$r_bb_3b_2$	3	3/10	(r_{bH})←<b_3>; (r_{bL})←<b_2>, load double registers BC, DE, HL, or SP immediate with bytes 3, 2, respectively.
MVI	M,b_2	2	3/10	(M)←<b_2>, store immediate byte 2 in the address specified by HL
MVI	r_ab_2	2	2/7	(r_a)←<b_2>, load register r_a immediate with byte 2 of the instruction.
MOV	Mr_a	1	2/7	(M)←(r_a), store register r_a in the memory location addressed by H and L.
MOV	r_aM	1	2/7	(r_a)←(M), load register r_a with contents of memory addressed by HL.
MOV	$r_{a1}r_{a2}$	1	1/5	(r_{a1})←(r_{a2}), load register r_{a1} with contents of r_{a2}, r_{a2} contents remain unchanged.
SHLD	b_3b_2	3	5/16	[<b_3> <b_2>]←(L); [<b_3> <b_2>+1)]←(H), store the contents of H and L into two successive memory locations specified by bytes 3 and 2.
XCHG		1	1/4	(H)−(D); (L)↔(E), exchange double registers HL and DE
XTHL		1	5/18	(L)−[(SP)], (H)↔[(SP)+1], (SP)=(SP), exchange the top of the stack with register HL.

2.3 INSTRUCTION SET OPCODES ALPHABETICALLY LISTED

MNEMONIC	BYTES	DESCRIPTION	REGISTER AFFECTED	POSITIVE-LOGIC HEX OPCODE D7–D4	POSITIVE-LOGIC HEX OPCODE D3–D0	CLOCK CYCLES*
ACI	2	Add immediate to A with carry†		C	E	7
ADC M	1	Add memory to A with carry†		8	E	7
ADC r	1	Add register to A with carry†	B	8	8	4
			C	8	9	
			D	8	A	
			E	8	B	
			H	8	C	
			L	8	D	
			A	8	F	
ADD M	1	Add memory to A†		8	6	7
ADD r	1	Add register to A†	B	8	0	4
			C	8	1	
			D	8	2	
			E	8	3	
			H	8	4	
			L	8	5	
			A	8	7	
ADI	2	Add immediate to A†		C	6	7
ANA M	1	AND memory with A†		A	6	7
ANAr	1	AND register with A†	B	A	0	4
			C	A	1	
			D	A	2	
			E	A	3	
			H	A	4	
			L	A	5	
			A	A	7	
ANI	2	AND immediate with A†		E	6	7
CALL	3	Call unconditional		C	D	17
CC	3	Call on carry		D	C	11/17
CM	3	Call on minus		F	C	11/17
CMA	1	Complement A		2	F	4
CMC	1	Complement carry‡		3	F	4
CMP M	1	Compare memory with A†		B	E	7
CMP r	1	Compare register with A				
			B	B	8	4
			C	B	9	
			D	B	A	
			E	B	B	
			H	B	C	
			L	B	D	
			A	B	F	
CNC	3	Call on no carry		D	4	11/17
CNZ	3	Call on no zero		C	4	11/17
CP	3	Call on positive		F	4	11/17
CPE	3	Call on parity even		E	C	11/17
CPI	2	Compare immediate with A†		F	E	7
CPO	3	Call on parity odd		E	4	11/17
CZ	3	Call on zero		C	C	11/17
DAA	1	Decimal adjust A†		2	7	4

*Two possible cycle times (11/17) indicate instruction cycles dependent on condition flags.
†All flags (C, Z, S, P, C1) affected.
‡Only carry flag affected.

MNEMONIC	BYTES	DESCRIPTION	REGISTER AFFECTED	POSITIVE-LOGIC HEX OPCODE D7–D4	POSITIVE-LOGIC HEX OPCODE D3–D0	CLOCK CYCLES
DAD B	1	Add B&C to H&L‡		0	9	10
DAD D	1	Add D&E to H&L‡		1	9	10
DAD H	1	Add H&L to H&L‡		2	9	10
DAD SP	1	Add stack pointer to H&L‡		3	9	10
DCR M	1	Decrement Memory§		3	5	10
DCR r	1	Decrement Register§	B	0	5	5
			C	0	D	
			D	1	5	
			E	1	D	
			H	2	5	
			L	2	D	
			A	3	D	
DCX B	1	Decrement B&C		0	B	5
DCX D	1	Decrement D&E		1	B	5
DCX H	1	Decrement H&L		2	B	5
DCX SP	1	Decrement stack pointer		3	B	5
DI	1	Disable interrupts		F	3	4
EI	1	Enable interrupts		F	B	4
HLT	1	Halt		7	6	7
IN	2	Input		D	B	10
INR M	1	Increment memory§		3	4	10
INR r	1	Increment register§	B	0	4	5
			C	0	C	
			D	1	4	
			E	1	C	
			H	2	4	
			L	2	C	
			A	3	C	
INX B	1	Increment B&C register		0	3	5
INX D	1	Increment D&E register		1	3	5
INX H	1	Increment H&L register		2	3	5
INX SP	1	Increment stack pointer		3	3	5
JC	3	Jump on carry		D	A	10
JM	3	Jump on minus		F	A	10
JMP	3	Jump unconditional		C	3	10
JNC	3	Jump on no carry		D	2	10
JNZ	3	Jump on no zero		C	2	10
JP	3	Jump on positive		F	2	10
JPE	3	Jump on parity even		E	A	10
JPO	3	Jump on parity odd		E	2	10
JZ	3	Jump on zero		C	A	10
LDA	1	Load A direct		3	A	13
LDAX B	1	Load A indirect		0	A	7
LDAX D	1	Load A indirect		1	A	7
LHLD	3	Load H&L direct		2	A	16
LXI B	3	Load immediate register pair B&C		0	1	10
LXI D	3	Load immediate register pair D&E		1	1	10
LXI H	3	Load immediate register		2	1	10
LXI SP	3	Load immediate stack pointer		3	1	10

‡Only carry flag affected.
§All flags except carry affected.

MNEMONIC	BYTES	DESCRIPTION	REGISTER AFFECTED	POSITIVE-LOGIC HEX OPCODE D7–D4	POSITIVE-LOGIC HEX OPCODE D3–D0	CLOCK CYCLES
MOV M,r	1	Move register to memory	B	7	0	7
			C	7	1	
			D	7	2	
			E	7	3	
			H	7	4	
			L	7	5	
			A	7	7	
MOV r,M	1	Move memory to register	B	4	6	7
			C	4	E	
			D	5	6	
			E	5	E	
			H	6	6	
			L	6	E	
			A	7	E	
MOV r_1, r_2	1	Move register to register	B,B	4	0	5
			B,C	4	1	
			B,D	4	2	
			B,E	4	3	
			B,H	4	4	
			B,L	4	5	
			B,A	4	7	
			C,B	4	8	
			C,C	4	9	
			C,D	4	A	
			C,E	4	B	
			C,H	4	C	
			C,L	4	D	
			C,A	4	F	
			D,B	5	0	
			D,C	5	1	
			D,D	5	2	
			D,E	5	3	
			D,H	5	4	
			H,L	5	5	
			D,A	5	7	
			E,B	5	8	
			E,C	5	9	
			E,D	5	A	
			E,E	5	B	
			E,H	5	C	
			E,L	5	D	
			E,A	5	F	
			H,B	6	0	
			H,C	6	1	
			H,D	6	2	
			H,E	6	3	
			H,H	6	4	
			H,L	6	5	
			H,A	6	7	
			L,B	6	8	

MNEMONIC	BYTES	DESCRIPTION	REGISTER AFFECTED	POSITIVE-LOGIC HEX OPCODE D7–D4	POSITIVE-LOGIC HEX OPCODE D3–D0	CLOCK CYCLES*
MOV r_1, r_2	1	Move register to register (continued)	L,C	6	9	
			L,D	6	A	
			L,E	6	B	
			L,H	6	C	
			L,L	6	D	
			L,A	6	F	
			A,B	7	8	
			A,C	7	9	
			A,D	7	A	
			A,E	7	B	
			A,H	7	C	
			A,L	7	D	
			A,A	7	F	
MVI M	2	Move immediate memory		3	6	10
MVI r	2	Move immediate register	B	0	6	7
			C	0	E	
			D	1	6	
			E	1	E	
			H	2	6	
			L	2	E	
			A	3	E	
NOP	1	No operation	4	0	0	4
ORA M	1	OR memory with A†		B	6	7
ORA r	1	OR register with A†	B	B	0	4
			C	B	1	
			D	B	2	
			E	B	3	
			H	B	4	
			L	B	5	
			A	B	7	
ORI	2	OR immediate with A†		F	6	7
OUT	2	Output		D	3	10
PCHL	1	H&L to program counter		E	9	5
POP B	1	Pop register pair B&C off stack		C	1	10
POP D	1	Pop register pair D&E off stack		D	1	10
POP H	1	Pop register pair H&L off stack		E	1	10
POP PSW	1	Pop A and flags off stack†		F	1	10
PUSH B	1	Push register pair B&C		C	5	11
PUSH D	1	Push register pair D&C		D	5	11
PUSH H	2	Push register pair H&L on stack		E	5	11
PUSH PSW	1	Push A and Flags on stack		F	5	11
RAL	1	Rotate A left through carry ‡		1	7	4
RAR	1	Rotate A right through carry‡		1	F	4
RC	1	Return on carry		D	8	5/11
RET	1	Return		C	9	10
RLC	1	Rotate A left‡		0	7	4
RM	1	Return on minus		F	8	5/11
RNC	1	Return on no carry		D	0	5/11
RNZ	1	Return on no zero		C	0	5/11
RP	1	Return on positive		F	0	5/11

*Two possible cycles times (11/17) indicate instruction cycles dependent on condition flags.
†All flags (C, Z, S, P, C1) affected.
‡Only carry flag affected.

MNEMONIC	BYTES	DESCRIPTION	REGISTER AFFECTED	POSITIVE-LOGIC HEX OPCODE D7–D4	POSITIVE-LOGIC HEX OPCODE D3–D0	CLOCK CYCLES*
RPE	1	Return on parity even		E	8	5/11
RPO	1	Return on parity odd		E	0	5/11
RRC	1	Rotate A right‡		0	F	4
RST	1	Restart				11
			$PC \leftarrow 0000_{16}$	C	7	
			$PC \leftarrow 0008_{16}$	C	F	
			$PC \leftarrow 0010_{16}$	D	7	
			$PC \leftarrow 0018_{16}$	D	F	
			$PC \leftarrow 0020_{16}$	E	7	
			$PC \leftarrow 0028_{16}$	E	F	
			$PC \leftarrow 0030_{16}$	F	7	
			$PC \leftarrow 0038_{16}$	F	F	
RZ	1	Return on Zero		C	8	5/11
SBB M	1	Subtract memory from A with borrow†		9	E	7
SBB r	1	Subtract register from A with borrow†	B	9	8	4
			C	9	9	
			D	9	A	
			E	9	B	
			H	9	C	
			L	9	D	
			A	9	F	
SBI	2	Subtract immediate from A with borrow†		D	E	7
SHLD	3	Store H&L direct		2	2	16
SPHL	1	H&L to stack pointer		F	9	5
STA	3	Store A direct		3	2	13
STAX B	1	Store A indirect		0	2	7
STAX D	1	Store A indirect		1	2	7
STC	1	Set carry‡		3	7	4
SUB M	1	Subtract memory from A†		9	6	7
SUB r	1	Subtract register from A†	B	9	0	4
			C	9	1	
			D	9	2	
			E	9	3	
			H	9	4	
			L	9	5	
			A	9	7	
SUI	2	Subtract immediate from A†		D	6	7
XCHG	1	Exchange D&E, H&L registers		E	B	4
XRA M	1	Exclusive OR memory with A†		A	E	7
XRA r	1	Exclusive OR register with A†	B	A	8	4
			C	A	9	
			D	A	A	
			E	A	B	
			H	A	C	
			L	A	D	
			A	A	F	
XRI	2	Exclusive OR immediate with A†		E	E	7
XTHL	1	Exchange top of stack H&L		E	3	18

*Two possible cycles times (11/17) indicate instruction cycles dependent on condition flags.
†All flags (C, Z, S, P, C1) affected.
‡Only carry flag affected.

3. TMS 8080 ELECTRICAL AND MECHANICAL SPECIFICATIONS

3.1 ABSOLUTE MAXIMUM RATINGS OVER OPERATING FREE-AIR TEMPERATURE RANGE (UNLESS OTHERWISE NOTED)*

Supply voltage, V_{CC} (see Note 1)	−0.3 V to 20 V
Supply voltage, V_{DD} (see Note 1	−0.3 V to 20 V
Supply voltage, V_{SS} (see Note 1)	−0.3 V to 20 V
All input and output voltages (see Note 1)	−0.3 V to 20 V
Continuous power dissipation	1.5 W
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Under absolute maximum ratings voltage values are with respect to the normally most negative supply voltage, V_{BB} (substrate). Throughout the remainder of this data sheet, voltage values are with respect to V_{SS} unless otherwise noted.

3.2 RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply voltage, V_{BB}	−4.75	−5	−5.25	V
Supply voltage, V_{CC}	4.75	5	5.25	V
Supply voltage, V_{DD}	11.4	12	12.6	V
Supply voltage, V_{SS}		0		V
High-level input voltage, V_{IH} (all inputs except clocks) (see Note 2)	3.3		V_{CC}+1	V
High-level clock input voltage, $V_{IH(\phi)}$	V_{DD}−1		V_{DD}+1	V
Low-level input voltage, V_{IL} (all inputs except clocks) (see Note 3)	−1		0.8	V
Low-level clock input voltage, $V_{IL(\phi)}$ (see Note 3)	−1		0.6	V
Operating free-air temperature, T_A	0		70	C

3.3 ELECTRICAL CHARACTERISTICS OVER FULL RANGE OF RECOMMENDED OPERATING CONDITIONS (UNLESS OTHERWISE NOTED)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
I_I	Input current (any input except clocks and data bus)	V_I = 0 V to V_{CC}			±10	μA
$I_{I(\phi)}$	Clock input current	$V_{I(\phi)}$ = 0 V to V_{DD}			±10	μA
$I_{I(DB)}$	Input current, data bus	$V_{I(DB)}$ = 0 V to V_{CC}			−100	μA
$I_{I(hold)}$	Address or data bus input current during hold	$V_{I(ad)}$ or $V_{I(DB)}$ = V_{CC}			10	μA
		$V_{I(ad)}$ or $V_{I(DB)}$ = 0 V			−100	
V_{OH}	High-level output voltage	I_{OH} = 100 μA	3.7			V
V_{OL}	Low-level output voltage	$I_{OL(DB)}$ = 1.7 mA, I_{OL} = 0.75 mA (any output except DB)			0.45	V
$I_{BB(av)}$	Average supply current from V_{BB}	Operating at $t_{c(\phi)}$ = 480 ns, T_A = 25°C		−0.01	−1	mA
$I_{CC(av)}$	Average supply current from V_{CC}			60	75	
$I_{DD(av)}$	Average supply current from V_{DD}			40	67	
C_i	Capacitance, any input except clock	V_{CC} = V_{DD} = V_{SS} = 0 V, V_{BB} = −4.75 to −5.25 V, f = 1 MHz, All other pins at 0 V		10	20	pF
$C_{i(\phi)}$	Clock input capacitance			5	10	
C_o	Output capacitance			10	20	

† All typical values are at T_A = 25°C and nominal voltages.

NOTES: 2. Active pull up resistors of nominally 2 kΩ will be switched onto the data bus when DBIN is high and the data input voltage is more positive than V_{IH} min.

3. The algebraic convention where the most negative limit is designated as minimum is used in this specification for logic voltage levels only.

3.4 TIMING REQUIREMENTS OVER FULL RANGE OF RECOMMENDED OPERATING CONDITIONS (SEE FIGURE 2)

		MIN	MAX	UNIT
$t_{c(\phi)}$	Clock cycle time (see Note 5)	480	2000	ns
$t_{r(\phi)}$	Clock rise time	5	50	ns
$t_{f(\phi)}$	Clock fall time	5	50	ns
$t_{w(\phi1)}$	Pulse width, clock 1 high	60		ns
$t_{w(\phi2)}$	Pulse width, clock 2 high	220		ns
$t_{d(\phi1L-\phi2)}$	Delay time, clock 1 low to clock 2	0		ns
$t_{d(\phi2-\phi1)}$	Delay time, clock 2 to clock 1	70		ns
$t_{d(\phi1H-\phi2)}$	Delay time, clock 1 high to clock 2 (time between leading edges)	130		ns
$t_{su(da-\phi1)}$	Data setup time with respect to clock 1	50		ns
$t_{su(da-\phi2)}$	Data setup time with respect to clock 2	150		ns
$t_{su(hold)}$	Hold input setup time	140		ns
$t_{su(int)}$	Interrupt input setup time	180		ns
$t_{su(rdy)}$	Ready input setup time	120		ns
$t_{h(da)}$	Data hold time (see Note 6)	$t_{PD(DBI)}$		ns
$t_{h(hold)}$	Hold input hold time	0		ns
$t_{h(int)}$	Interrupt input hold time	0		ns
$t_{h(rdy)}$	Ready input hold time	0		ns

NOTES: 5. $t_{c(\phi)} = t_{d(\phi1L-\phi2)} + t_{r(\phi2)} + t_{w(\phi2)} + t_{f(\phi2)} + t_{d(\phi2-\phi1)} + t_{r(\phi1)}$. 480 ns $\leqslant t_{c(\phi)} \leqslant$ 2000 ns.
6. The data input should be enabled using the DBIN status signal. No bus conflict can then occur and the data hold time requirement is thus assured.

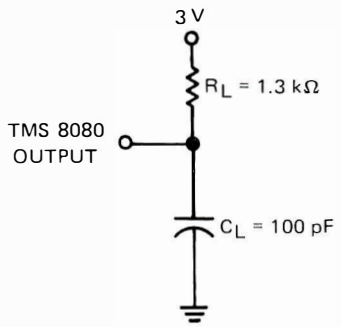
3.5 SWITCHING CHARACTERISTICS OVER FULL RANGE OF RECOMMENDED OPERATING CONDITIONS (SEE FIGURE 2)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$t_{PD(ad)}$	Propagation delay time, clock 2 to address outputs	C_L = 100 pF, R_L = 1.3 kΩ		200	ns
$t_{PD(da)}$	Propagation delay time, clock 2 to data bus			220	ns
$t_{PD(cont)}$	Propagation delay time, clocks to control outputs			120	ns
$t_{PD(DBI)}$	Propagation delay time, clock 2 to DBIN output		25	140	ns
$t_{PD(int)}$	Propagation delay time, clock 2 to INTE output			200	ns
t_{DI}	Time for data bus to enter input mode			$t_{PD(DBI)}$	ns
t_{PXZ}	Disable time to high-impedance state during hold (address outputs and data bus)			120	ns

The time that the address outputs and output data will remain stable after $\overline{WR}$ goes high, t_{WA} and $t_{WD} \geqslant t_{d(\phi1H-\phi2)}$.
The time between address outputs becoming stable and $\overline{WR}$ going low, $t_{AW} \leqslant 2\,t_{c(\phi)} - t_{d(\phi1H-\phi2)} - t_{r(\phi)} - 120$ ns.
The time between output data becoming stable and $\overline{WR}$ going low, $t_{DW} \geqslant t_{c(\phi)} - t_{d(\phi1H-\phi2)} - t_{r(\phi)} - 150$ ns.
The following are relevant when interfacing to devices requiring V_{IH} min of 3.3 V:

a) Maximum output rise time (t_{TLH}) from 0.8 V to 3.3 V is 140 ns with C_L as specified for the propagation delay times above.

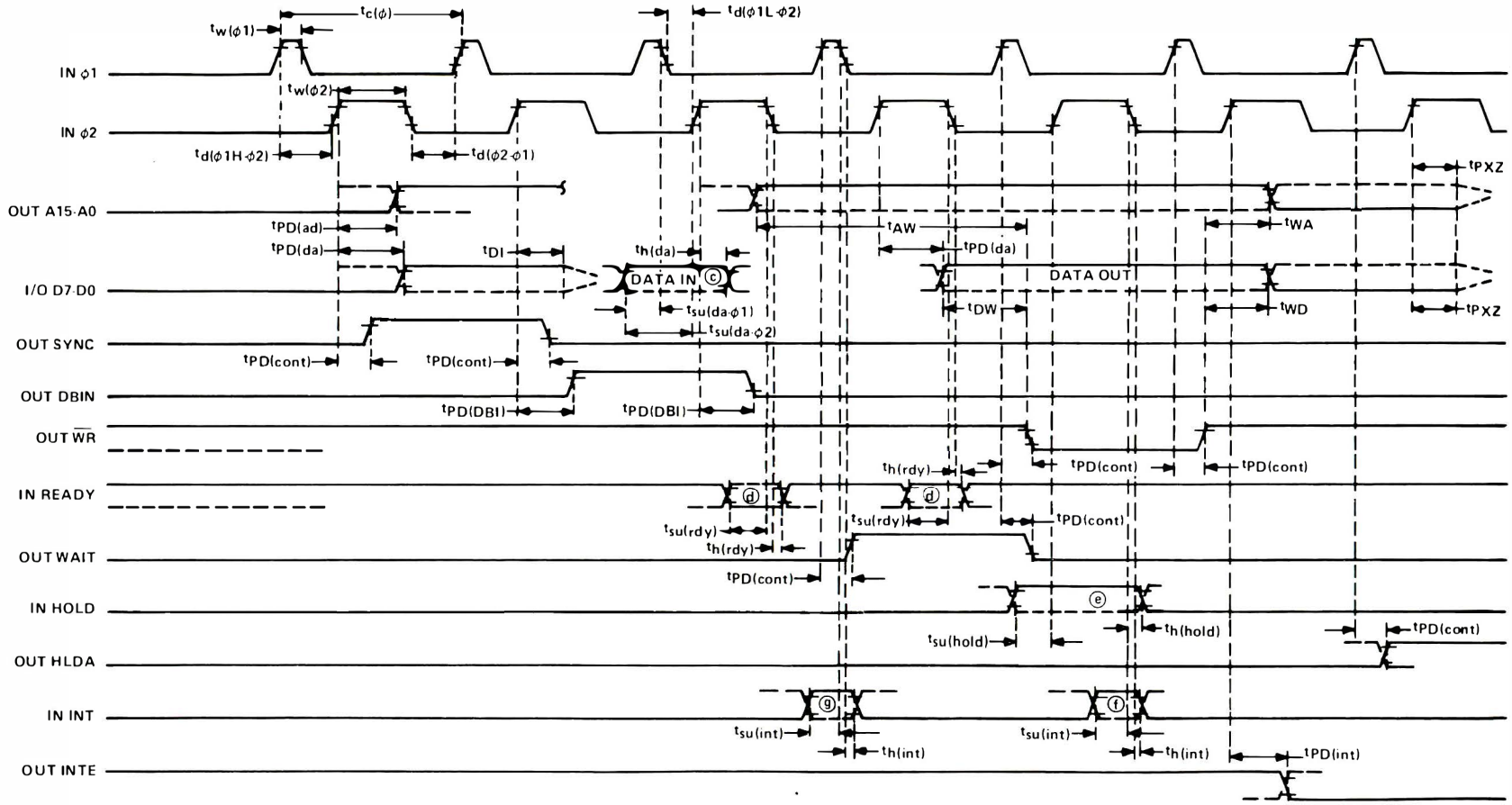
b) Maximum propagation delay times when measured to $V_{ref(H)}$ = 3 V (instead of 2 V) will be 60 ns more than as specified above with C_L as specified.



C_L includes probe and jig capacitance.

LOAD CIRCUIT

voltage waveforms (see notes a and b)



NOTES: a. This timing diagram shows timing relationships only, it does not represent any specific machine cycle.

b. Time measurements are made at the following reference voltages: Clock, $V_{ref(H)}$ = 9.5 V, $V_{ref(L)}$ = 1 V. Other inputs, $V_{ref(H)}$ = 2 V, $V_{ref(L)}$ = 0.8 V.

c. Data in must be stable for this period when DBIN is high during S3. Requirements for both $t_{su(da\text{-}\phi1)}$ and $t_{su(da\text{-}\phi2)}$ must be satisfied.

d. The ready signal must be stable for this period during S2 or SW. This requires external synchronization.

e. The hold signal must be stable for this period during S2 or SW when entering the hold mode and during S3, S4, S5 and SWH when in the hold mode. This requires external synchronization.

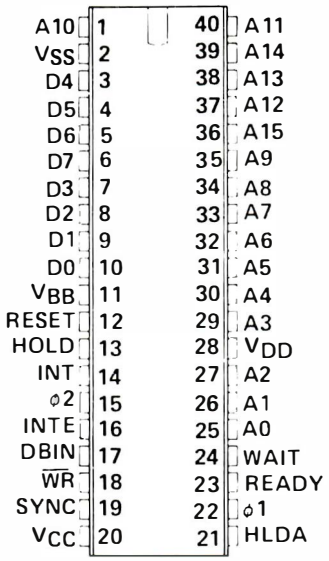
f. The interrupt signal must be stable during this period on the last clock cycle of any instruction to be recognized on the following instruction. External synchronization is not required.

g. During halt mode only, timing is with respect to the clock 1 falling edge.

FIGURE 2

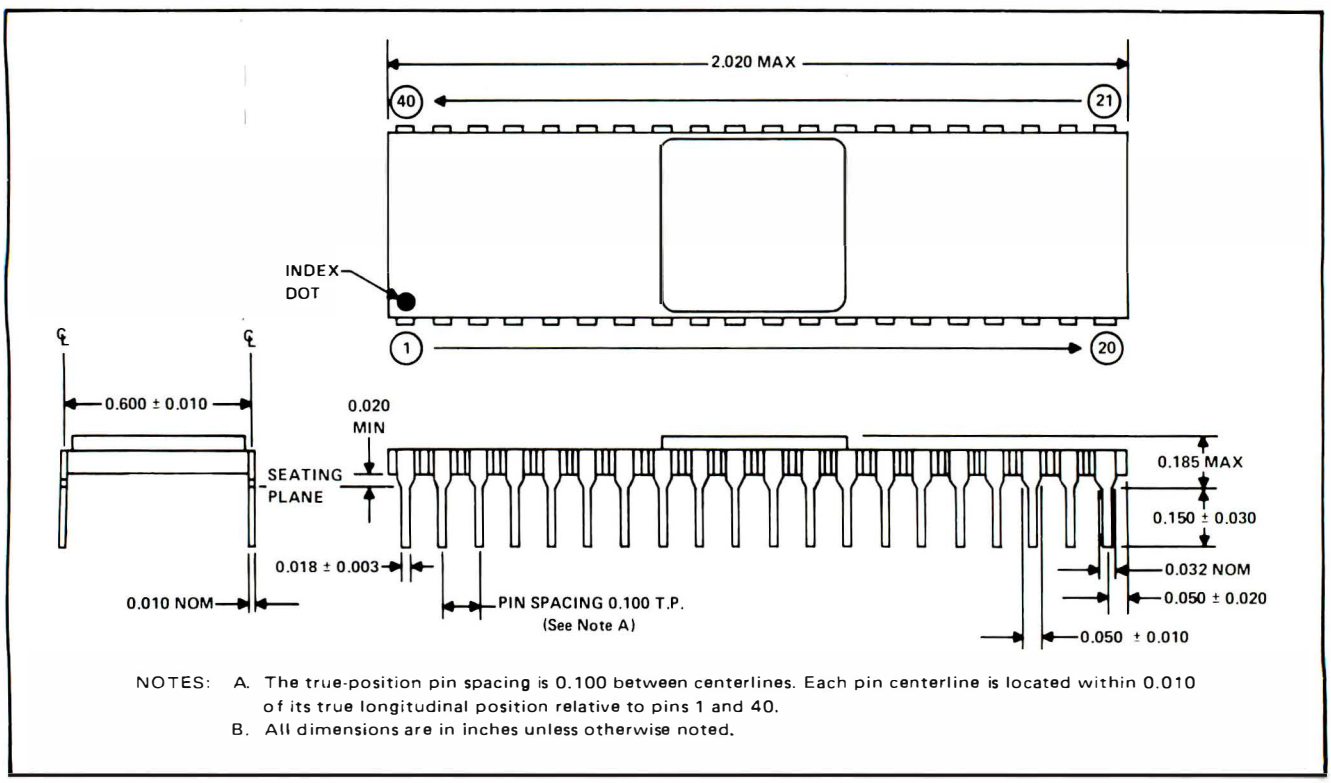
3.6 TERMINAL ASSIGNMENTS

TMS 8080



3.7 MECHANICAL DATA

40-PIN CERAMIC PACKAGE



NOTES: A. The true-position pin spacing is 0.100 between centerlines. Each pin centerline is located within 0.010 of its true longitudinal position relative to pins 1 and 40.
B. All dimensions are in inches unless otherwise noted.

APPENDIX B
TMS 5501 MULTIFUNCTION INPUT/OUTPUT CONTROLLER

Appendix B

TMS 5501 Multifunction Input/Output Controller

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

TMS 5501 MULTIFUNCTION INPUT/OUTPUT CONTROLLER

1. INTRODUCTION

1.1 DESCRIPTION

The TMS 5501 is a multifunction input/output circuit for use with TI's TMS 8080 CPU. It is fabricated with the same N-channel silicon-gate process as the TMS 8080 and has compatible timing, signal levels, and power supply requirements. The TMS 5501 provides a TMS 8080 microprocessor system with an asynchronous communications interface, data I/O buffers, interrupt control logic, and interval timers.

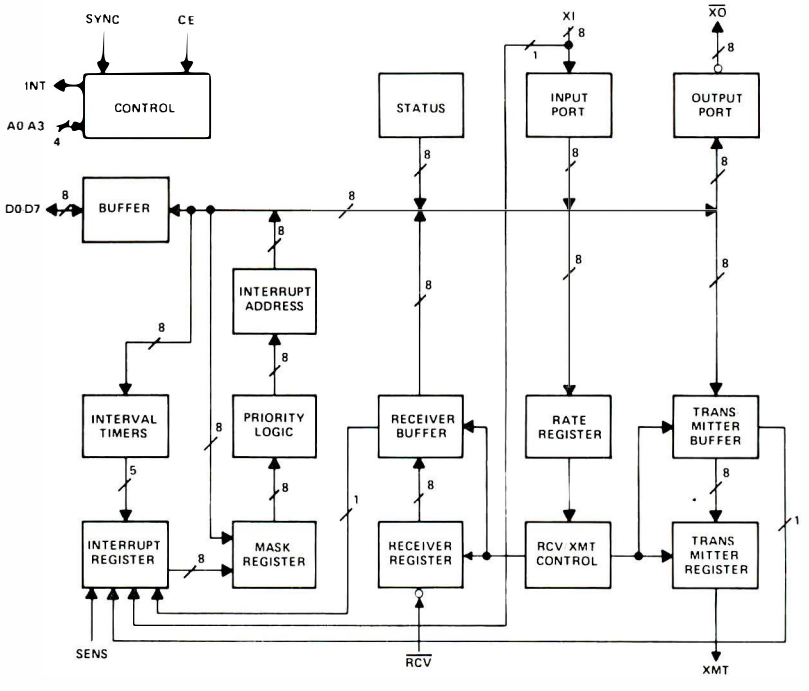


FIGURE 1–TMS 5501 BLOCK DIAGRAM

The I/O section of the TMS 5501 contains an eight-bit parallel input port and a separate eight-bit parallel output port with storage register. Five programmable interval timers provide time intervals from 64 μs to 16.32 ms.

The interrupt system allows the processor to effectively communicate with the interval timers, external signals, and the communications interface by providing TMS 8080-compatible interrupt logic with masking capability.

Data transfers between the TMS 5501 and the CPU are carried by the data bus and controlled by the interrupt, chip enable, sync, and address lines. The TMS 8080 uses four of its memory-address lines to select one of 14 commands to which the TMS 5501 will respond. These commands allow the CPU to:

---- read the receiver buffer
---- read the input port
---- read the interrupt address
---- read TMS 5501 status
---- issue discrete commands
---- load baud rate register
---- load the transmitter buffer
---- load the output port
---- load the mask register
---- load an interval timer

The commands are generated by executing memory referencing instructions such as MOV (register to memory) with the memory address being the TMS 5501 command. This provides a high degree of flexibility for I/O operations by letting the systems programmer use a variety of instructions.

1.2 SUMMARY OF OPERATION

Addressing the TMS 5501

A convenient method for addressing the TMS 5501 is to tie the chip enable input to the highest order address line of the CPU's 16-bit address bus and the four TMS 5501 address inputs to the four lowest order bits of the bus. This, of course, limits the system to 32,768 words of memory but in many applications the full 65,536 word memory addressing capability of the TMS 8080 is not required.

Communications Functions

The communications section of the TMS 5501 is an asynchronous transmitter and receiver for serial communications and provides the following functions:

Programmable baud rate – A CPU command selects a baud rate of 110, 150, 300, 1200, 2400, 4800, or 9600 baud.

Incoming character detection – The receiver detects the start and stop bits of an incoming character and places the character in the receive buffer.

Character transmission – The transmitter generates start and stop bits for a character received from the CPU and shifts it out.

Status and command signals – Via the data bus, the TMS 5501 signals the status of: framing error and overrun error flags; data in the receiver and transmitter buffers; start and data bit detectors; and end-of-transmission (break) signals from external equipment. It also issues break signals to external equipment.

Data Interface

The TMS 5501 moves data between the CPU and external devices through its internal data bus, input port, and output port. When data is present on the bus that is to be sent to an external device, a Load Output Port (LOP) command from the CPU puts the data on the $\overline{XO}$ pins of the TMS 5501 by latching it in the output port. The data remains in the port until another LOP command is received. When the CPU requires data that is present on the External Input (XI) lines, it issues a command that gates the data onto the internal data bus of the TMS 5501 and consequently onto the CPU's data bus at the correct time during the CPU cycles.

Interval Timers

To start a countdown by any of the five interval timers, the program selects the particular timer by an address to the TMS 5501 and loads the required interval into the timer via the data bus. Loading the timer activates it and it counts down in increments of 64 microseconds. The 8-bit counters provide intervals that vary in duration from 64 to 16,320 microseconds. Much longer intervals can be generated by cascading the timers through software. When a timer reaches zero, it generates an interrupt that typically will be used to point to a subroutine that performs a servicing function such as polling a peripheral or scanning a keyboard. Loading an interval value of zero causes an immediate interrupt. A new value loaded while the interval timer is counting overrides the previous value and the interval timer starts counting down the new interval. When an interval timer reaches zero it remains inactive until a new interval is loaded.

Servicing Interrupts

The TMS 5501 provides a TMS 8080 system with several interrupt control functions by receiving external interrupt signals, generating interrupt signals, masking out undersired interrupts, establishing the priority of interrupts, and generating RST instructions for the TMS 8080. An external interrupt is received on pin 22, SENS. An additional external interrupt can be received on pin 32, XI7, if selected by a discrete command from the TMS 8080 (See Figure 4). The TMS 5501 generates an interrupt when any of the five interval timers count to zero. Interrupts are also generated when the receiver buffer is loaded and when the transmitter buffer is empty.

When an interrupt signal is received by the interrupt register from a particular source, a corresponding bit is set and gated to the mask register. A pattern will have previously been set in the mask register by a load-mask-register command from the TMS 8080. This pattern determines which interrupts will pass through to the priority logic. The priority logic allows an interrupt to generate an RST instruction to the TMS 8080 only if there is no higher priority interrupt that has not been accepted by the TMS 8080. The TMS 5501 prioritizes interrupts in the order shown below:

1st – Interval Timer #1
2nd – Interval Timer #2
3rd – External Sensor
4th – Interval Timer #3
5th – Receiver Buffer Loaded
6th – Transmitter Buffer Emptied
7th – Interval Timer #4
8th – Interval Timer #5 or an External Input (XI 7)

The highest priority interrupt passes through to the interrupt address logic, which generates the RST instruction to be read by the TMS 8080. See Table 3 for relationship of interrupt sources to RST instructions and Figures 6 and 8 for timing relationships.

The TMS 5501 provides two methods of servicing interrupts; an interrupt-driven system or a polled-interrupt system. In an interrupt-driven system, the INT signal of the TMS 5501 is tied to the INT input of the TMS 8080. The sequence of events will be: (1) The TMS 5501 receives (or generates) an interrupt signal and readies the appropriate RST instruction. (2) The TMS 5501 INT output, tied to the TMS 8080 INT input, goes high signaling the TMS 8080 that an interrupt has occured. (3) If the TMS 8080 is enabled to accept interrupts, it sets the INTA (interrupt acknowledge) status bit high at SYNC time of the next machine cycle. (4) If the TMS 5501 has previously received an interrupt-acknowledge-enable command from the CPU (see Bit 3, Paragraph 2.2.5), the RST instruction is transferred to the data bus.

In a polled-interrupt system, INT is not used and the sequence of events will be: (1) The TMS 5501 receives (or generates) an interrupt and readies the RST instruction. (2) The TMS 5501 interrupt-pending status bit (see Bit 5, Paragraph 2.2.4) is set high (the interrupt-pending status bit and the INT output go high simultaneously). (3) At the prescribed time, the TMS 8080 polls the TMS 5501 to see if an interrupt has occurred by issuing a read-TMS 5501-status command and reading the interrupt-pending bit. (4) If the bit is high, the TMS 8080 will then issue a read-interrupt-address command, which causes the TMS 5501 to transfer the RST instruction to the data bus as data for the instruction being executed by the TMS 8080.

1.3 APPLICATIONS

Communications Terminals

The functions of the TMS 5501 make it particularly useful in TMS 8080-based communications terminals and generally applicable in systems requiring periodic or random servicing of interrupts, generation of control signals to external devices, buffering of data, and transmission and reception of asynchronous serial data. As an example, a system configuration such as shown in Figure 2 can function as the controller for a terminal that governs employee entrance into a plant or security areas within a plant. Each terminal is identified by a central computer through ID switches. The central system supplies each terminal's RAM with up to 16 employee access categories applicable to that terminal. These categories are compared with an employee's badge character when he inserts his badge into the badge sensor. If a

match is not found, a reject light will be activated. If a match is found, the terminal will transmit the employee's badge number and access category to the central system, and a door unlock solenoid will be activated for 4 seconds. The central computer then may take the transmitted information and record it along with time and date of access.

The TMS 4700 is a 1024 x 8 ROM that contains the system program, and the TMS 4036 is a 64 x 8 RAM that serves as the stack for the TMS 8080 and storage for the access category information. TTL circuits control chip-enable information carried by the address bus. Signals from the CPU gate the address bits from the ROM, the RAM, or the TMS 5501 onto the data bus at the correct time in the CPU cycle. The clock generator consists of four TTL circuits along with a crystal, needed to maintain accurate serial data assembly and disassembly with the central computer.

The TMS 5501 handles the asynchronous serial communication between the TMS 8080 and the central system and gates data from the badge reader onto the data bus. It also gates control and status data from the TMS 8080 to the door lock and badge reader and controls the time that the door lock remains open. The TMS 5501 signals the TMS 8080 when the badge reader or the communication lines need service. The functions that the TMS 5501 is to perform are selected by an address from the TMS 8080 with the highest order address line tied to the TMS 5501 chip enable input and the four lowest order lines tied to the address inputs.

2. OPERATIONAL AND FUNCTIONAL DESCRIPTION

This detailed description of the TMS 5501 consists of:

INTERFACE SIGNALS – a definition of each of the circuit's external connections

COMMANDS – the address required to select each of the TMS 5501 commands and a description of the response to the command.

2.1 INTERFACE SIGNALS

The TMS 5501 communicates with the TMS 8080 via four address lines: a chip enable line, an eight-bit bidirectional data bus, an interrupt line, and a sync line. It communicates with system components other than the CPU via eight external inputs, eight external outputs, a serial receiver input, a serial transmitter output, and an external sensor input. Table 1 defines the TMS 5501 pin assignments and describes the function of each pin.

TABLE 1
TMS 5501 PIN ASSIGNMENTS AND FUNCTIONS

SIGNATURE	PIN	DESCRIPTION
		INPUTS
CE	18	Chip enable—When CE is low, the TMS 5501 address decoding is inhibited, which prevents execution of any of the TMS 5501 commands.
A3	17	Address bus—A3 through A0 are the lines that are addressed by the TMS 8080 to select a particular
A2	16	TMS 5501 function.
A1	15	
A0	14	
SYNC	19	Synchronizing signal—The SYNC signal is issued by the TMS 8080 and indicates the beginning of a machine cycle and availability of machine status. When the SYNC signal is active (high), the TMS 5501 will monitor the data bus bits D0 (interrupt acknowledge) and D1 ($\overline{WO}$, data output function).
$\overline{RCV}$	5	Receiver serial data input line—$\overline{RCV}$ must be held in the inactive (high) state when not receiving data. A transition from high to low will activate the receive circuitry.

TABLE 1 (continued)
TMS 5501 PIN ASSIGNMENTS AND FUNCTIONS

SIGNATURE	PIN	DESCRIPTION
		INPUTS
XI 0	39	External inputs—These eight external inputs are gated to the data bus when the read-external-inputs function is addressed. External input n is gated to data bus bit n without conversion.
XI 1	38	
XI 2	37	
XI 3	36	
XI 4	35	
XI 5	34	
XI 6	33	
XI 7	32	
SENS	22	External interrupt sensing – A transition from low to high at SENS sets a bit in the interrupt register, which, if enabled, generates an interrupt to the TMS 8080.
		OUTPUTS
$\overline{XO}$ 0	24	External outputs—These eight external outputs are driven by the complement of the output register; i.e., if output register bit n is loaded with a high (low) from data bus bit n by a load-output register command, the external output n will be a low (high). The external outputs change only when a load-output-register function is addressed.
$\overline{XO}$ 1	25	
$\overline{XO}$ 2	26	
$\overline{XO}$ 3	27	
$\overline{XO}$ 4	28	
$\overline{XO}$ 5	29	
$\overline{XO}$ 6	30	
$\overline{XO}$ 7	31	
XMT	40	Transmitter serial data output line—This line remains high when the TMS 5501 is not transmitting.
		DATA BUS INPUT/OUTPUT
D0	13	Data bus – Data transfers between the TMS 5501 and the TMS 8080 are made via the 8-bit bidirectional data bus. D0 is the LSB. D7 is the MSB.
D1	12	
D2	11	
D3	10	
D4	9	
D5	8	
D6	7	
D7	6	
INT	23	Interrupt—When active (high), the INT output indicates that at least one of the interrupt conditions has occurred and that its corresponding mask-register bit is set.
		POWER AND CLOCKS
V_{SS}	4	Ground reference
V_{BB}	1	Supply voltage (−5 V nominal)
V_{CC}	2	Supply voltage (5 V nominal)
V_{DD}	3	Supply voltage (12 V nominal)
$\phi 1$	20	Phase 1 clock
$\phi 2$	21	Phase 2 clock

2.2 TMS 5501 COMMANDS

The TMS 5501 operates as input/output device for the TMS 8080. Functions are initiated via the TMS 8080 address bus and the TMS 5501 address inputs. Address decoding to determine the command function being issued is defined in Table 2.

TABLE 2
COMMAND ADDRESS DECODING
When Chip Enable Is High

#2 5501 PORT NO.	#1 5501 PORT NO.	A3	A2	A1	A0	COMMAND	FUNCTION	PARAGRAPH
16	0	L	L	L	L	Read receiver buffer	RBn → Dn	2.2.1
17	1	L	L	L	H	Read external inputs	XIn → Dn	2.2.2
18	2	L	L	H	L	Read interrupt address	RST → Dn	2.2.3
19	3	L	L	H	H	Read TMS 5501 status	(Status) → Dn	2.2.4
20	4	L	H	L	L	Issue discrete commands	See Fig.4	2.2.5
21	5	L	H	L	H	Load rate register	See Fig.4	2.2.6
22	6	L	H	H	L	Load transmitter buffer	Dn → TBn	2.2.7*
23	7	L	H	H	H	Load Output port	Dn → XOn	2.2.8
24	8	H	L	L	L	Load mask register	Dn → MRn	2.2.9
25	9	H	L	L	H	Load interval timer 1	Dn → Timer 1	2.2.10
26	10	H	L	H	L	Load interval timer 2	Dn → Timer 2	2.2.10
27	11	H	L	H	H	Load interval timer 3	Dn → Timer 3	2.2.10
28	12	H	H	L	L	Load interval timer 4	Dn → Timer 4	2.2.10
29	13	H	H	L	H	Load interval timer 5	Dn → Timer 5	2.2.10
30	14	H	H	H	L	No function		
31	15	H	H	H	H	No function		

* Important

RBn Receiver buffer bit n
Dn Data bus I/O terminal n
Xln External input terminal n
RST 11 ($1A_5$) ($1A_4$) ($1A_3$) 1 1 1 (see Table 3)
TBn Transmit buffer bit n
XOn Output register bit n
MRn Mask register bit n

TABLE 3
RST INSTRUCTIONS

DATA BUS BIT 0	1	2	3	4	5	6	7	INTERRUPT CAUSED BY	#1 TMS 5501
H	H	H	L	L	L	H	H	Interval Timer 1	Power Up
H	H	H	H	L	L	H	H	Interval Timer 2	User Timer
H	H	H	L	H	L	H	H	External Sensor	Keyboard
H	H	H	H	H	L	H	H	Interval Timer 3	Repeat Key
H	H	H	L	L	H	H	H	Receiver Buffer	Rx RS-232
H	H	H	H	L	H	H	H	Transmitter Buffer	Tx RS-232
H	H	H	L	H	H	H	H	Interval Timer 4	Bell Timer
H	H	H	H	H	H	H	H	Interval Timer 5 of X17	CRT Executive Loop

The following paragraphs define the functions of the TMS 5501 commands.

2.2.1 Read receiver buffer

Addressing the read-receiver-buffer function causes the receiver buffer contents to be transferred to the TMS 8080 and clears the receiver-buffer-loaded flag.

2.2.2 Read external input lines

Addressing the read-external-inputs function transfers the states of the eight external input lines to the TMS 8080.

2.2.3 Read interrupt address

Addressing the read interrupt address function transfers the current highest priority interrupt address onto the data bus as read data. After the read operation is completed, the corresponding bit in the interrupt register is reset.

If the read-interrupt-address function is addressed when there is no interrupt pending, a false interrupt address will be read. TMS 5501 status function should be addressed in order to determine whether or not an interrupt condition is pending.

2.2.4 Read TMS 5501 status

Addressing the read-TMS 5501-status function gates the various status conditions of the TMS 5501 onto the data bus. The status conditions, available as indicated in Figure 3, are described in the following paragraphs.

BIT:	7	6	5	4	3	2	1	0
	START BIT DETECT	FULL BIT DETECT	INTRPT PENDING	XMIT BUFFER EMPTY	RCV BUFFER LOADED	SERIAL RCVD	OVERRUN ERROR	FRAME ERROR

FIGURE 3–DATA BUS ASSIGNMENTS FOR TMS 5501 STATUS

Bit 0, framing error

A high in bit 0 indicates that a framing error was detected on the last character received (either one or both stop bits were in error). The framing error flag is updated at the end of each character. Bit 0 of the TMS 5501 status will remain high until the next valid character is received.

Bit 1, overrun error

A high in bit 1 indicates that a new character was loaded into the receiver buffer before a previous character was read out. The overrun error flag is cleared each time the read-I/O-status function is addressed or a reset command is issued.

Bit 2, serial received data

Bit 2 monitors the receiver serial data input line. This line is provided as a status input for use in detecting a break and for test purposes. Bit 2 is normally high when no data is being received.

Bit 3, receiver buffer loaded

A high in bit 3 indiciates that the receiver buffer is loaded with a new character. The receiver-buffer-loaded flag remains high until the read-receiver-buffer function is addressed (at which time the flag is cleared). The reset function also clears this flag.

Bit 4, transmitter buffer empty
A high in bit 4 indicates that the transmitter buffer register is empty and ready to accept a character. Note, however, that the serial transmitter register may be in the process of shifting out a character. The reset function sets the transmitter-buffer-empty flag high.

Bit 5, interrupt pending
A high in bit 5 indicates that one or more of the interrupt conditions has occured and the corresponding interrupt is enabled. This bit is the status of the interrupt signal INT.

Bit 6, full bit detected
A high in bit 6 indicates that the first data bit of a receive-data character has been detected. This bit remains high until the entire character has been received or until a reset is issued and is provided for test purposes.

Bit 7, start bit detected
A high in bit 7 indicates that the start bit of an incoming data character has been detected. This bit remains high until the entire character has been received or until a reset is issued and is provided for test purposes.

2.2.5 Issue discrete commands

Addressing the discrete command function causes the TMS 5501 to interpret the data bus information according to the following descriptions. See Figure 4 for the discrete command format. Bits 1 through 5 are latched until a different discrete command is received.

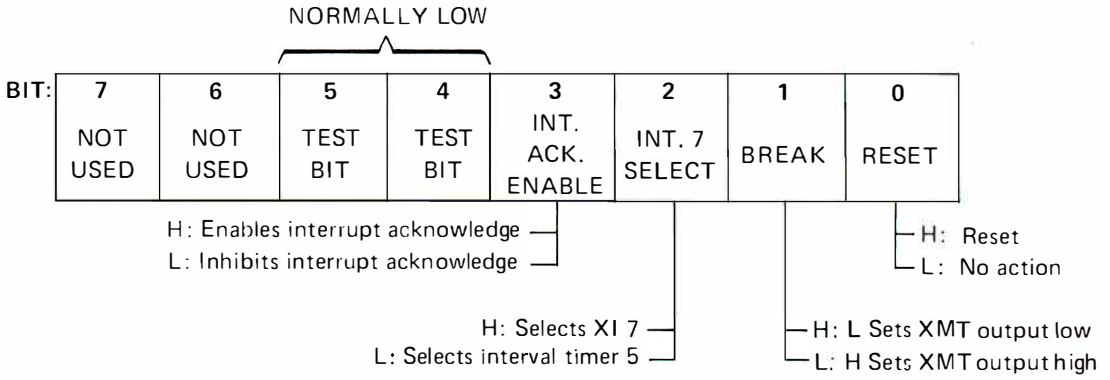


FIGURE 4–DISCRETE COMMAND FORMAT

Bit 0, reset
A high in bit 0 will cause the following:

1) The receiver buffer and register are cleared to the search mode including the receiver-buffer-loaded flag, the start-bit-detected flag, the full-bit-cletected flag, and the overrun-error flag. The receiver buffer is not cleared and will contain the last character received.
2) The transmitter data output is set high (marking). The transmitter-buffer-empty flag is set high indicating that the transmitter buffer is ready to accept a character from the TMS 8080.
3) The interrupt register is cleared except for the bit corresponding to the transmitter buffer interrupt, which is set high.
4) The interval timers are inhibited.

A low in bit 0 causes no action. The reset function has no affect on the output port, the external inputs, interrupt acknowledge enable, the mask register, the rate register, the transmitter register, or the transmitter buffer.

Bit 1, break
A low in bit 1 causes the transmitter data output to be reset low (spacing).

If bit 0 and bit 1 are both high, the reset function will override.

Bit 2, interrupt 7 select
Interrupt 7 may be generated either by a low to high transition of external input 7 or by interval timer 5.

A high in bit 2 selects the interrupt 7 source to be the transition of external input 7. A low in bit 2 selects the interrupt 7 source to be interval timer 5.

Bit 3, interrupt acknowledge enable
The TMS 5501 decodes data bus (CPU status) bit 0 at SYNC of each machine cycle to determine if an interrupt acknowledge is being issued.

A high in bit 3 enables the TMS 5501 to accept the interrupt acknowledge decode. A low in bit 3 causes the TMS 5501 to ignore the interrupt acknowledge decode.

Bit 4 and bit 5 are used only during testing of the TMS 5501. For correct system operation both bits must be kept low.

Bit 6 and bit 7 are not used and can assume any value.

2.2.6 Load rate register

Addressing the load-rate-register function causes the TMS 5501 to load the rate register from the data bus and interpret the data bits (See Figure 5) as follows.

BIT:	7	6	5	4	3	2	1	0
	STOP BIT(s)	9600 baud	4800 baud	2400 baud	1200 baud	300 baud	150 baud	110 baud

H: One stop bit
L: Two stop bits

FIGURE 5–DATA BUS ASSIGNMENTS FOR RATE COMMANDS

Bits 0 through 6, rate select

The rate select bits (bits 0 through 6) are mutually exclusive, i.e., only one bit may be high. A high in bits 0 through 6 will select the baud rate for both the transmitter and receiver circuitry as defined below and in Figure 5:

Bit 0 110 baud
Bit 1 150 baud
Bit 2 300 baud
Bit 3 1200 baud
Bit 4 2400 baud
Bit 5 4800 baud
Bit 6 9600 baud

If more than one bit is high, the highest rate indicated will result. If bits 0 through 6 are all low, both the receiver and the transmitter circuitry will be inhibited.

Bit 7, stop bits

Bit 7 determines whether one or two stop bits are to be used by both the transmitter and receiver circuitry. A high in bit 7 selects one stop bit. A low in bit 7 selects two stop bits.

2.2.7 Load transmitter buffer

Addressing the load-transmitter-buffer function transfers the state of the data bus into the transmitter buffer.

2.2.8 Load output port

Addressing the load-output-port function transfers the state of the data bus into the output port. The data is latched and remains on $\overline{XO\ 0}$ through $\overline{XO\ 7}$ as the complement of the data bus until new data is loaded.

2.2.9 Load mask register

Addressing the load-mask-register function loads the contents of the data bus into the mask register. A high in data bus bit n enables interrupt n. A low inhibits the corresponding interrupt.

2.2.10 Load timer n

Addressing the load-timer-n function loads the contents of the data bus into the appropriate interval timer. Time intervals of from 64 μs (data bus = LLLLLLLH) to 16,320 μs (data bus HHHHHHHH) are counted in 64-μs, steps. When the count of interval timer n reaches 0, the bit in the interrupt register that corresponds to timer n is set and an interrupt is generated. Loading all lows causes an interrupt immediately.

3. TMS 5501 ELECTRICAL AND MECHANICAL SPECIFICATIONS

3.1 ABSOLUTE MAXIMUM RATINGS OVER OPERATING FREE-AIR TEMPERATURE RANGE (UNLESS OTHERWISE NOTED)*

Supply voltage, V_{CC} (see Note 1)	−0.3 V to 20 V
Supply voltage, V_{DD} (see Note 1	−0.3 V to 20 V
Supply voltage, V_{SS} (see Note 1)	−0.3 V to 20 V
All input and output voltages (see Note 1)	−0.3 V to 20 V
Continuous power dissipation	1.1 W
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Under absolute maximum ratings voltage values are with respect to the normally most negative supply voltage, V_{BB} (substrate). Throughout the remainder of this data sheet, voltage values are with respect to V_{SS} unless otherwise noted.

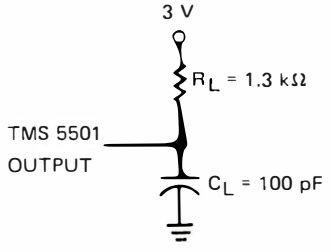
3.2 RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply voltage, V_{BB}	−4.75	−5	−5.25	V
Supply voltage, V_{CC}	4.75	5	5.25	V
Supply voltage, V_{DD}	11.4	12	12.6	V
Supply voltage, V_{SS}		0		V
High-level input voltage, V_{IH} (all inputs except clocks)	3.3		V_{CC}+1	V
High-level clock input voltage, $V_{IH(\phi)}$	V_{DD}−1		V_{DD}+1	V
Low-level input voltage, V_{IL} (all inputs except clocks) (see Note 2)	−1		0.8	V
Low-level clock input voltage, $V_{IL(\phi)}$ (see Note 2)	−1		0.6	V
Operating free-air temperature, T_A	0		70	°C

NOTE 2: The algebraic convention where the most negative limit is designated as minimum is used in this specification for logic voltage levels only.

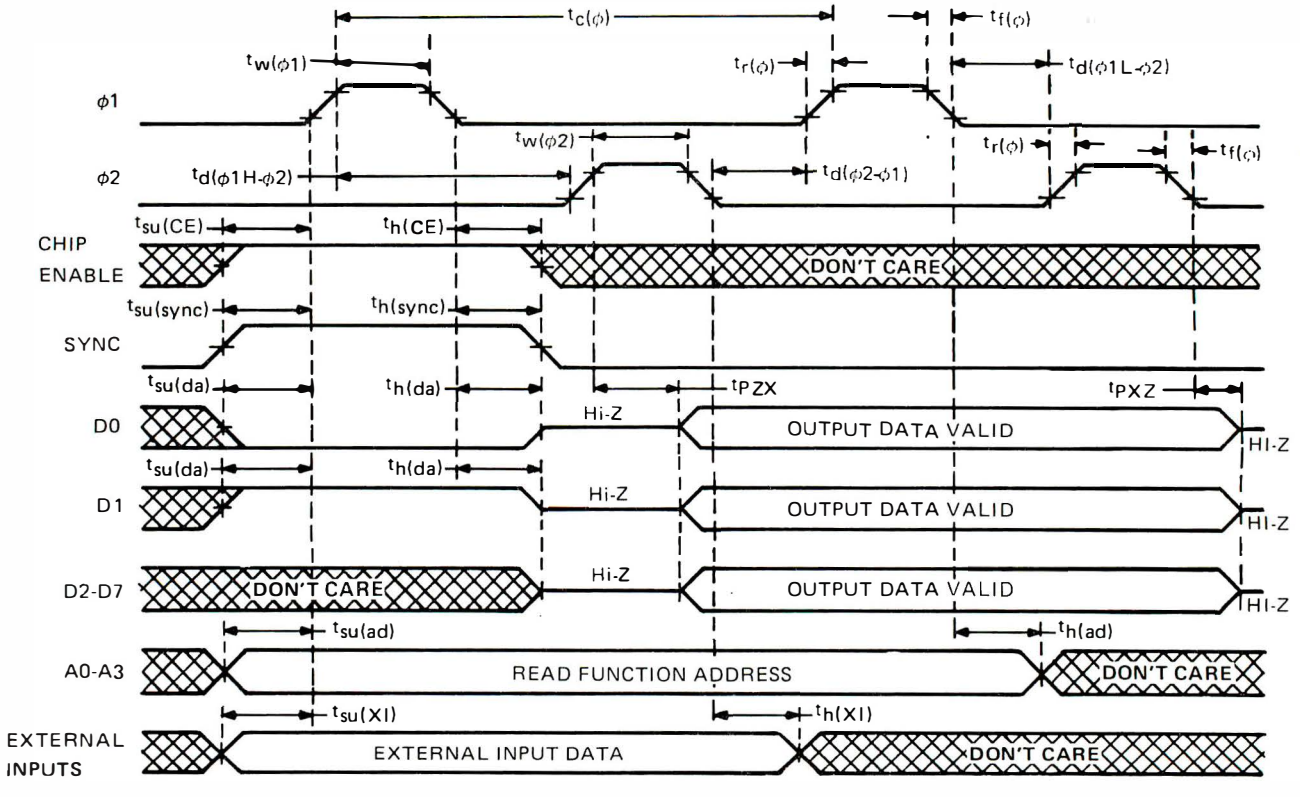
3.5 SWITCHING CHARACTERISTICS OVER FULL RANGE OF RECOMMENDED OPERATING CONDITIONS (SEE FIGURES 6 AND 7)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{PZX}	Data bus output enable time	C_L = 100 pF, R_L = 1.3 kΩ		200	ns
t_{PXZ}	Data bus output disable time to high-impedance state			180	ns
t_{PD}	External data output propagation delay time from φ2			200	ns



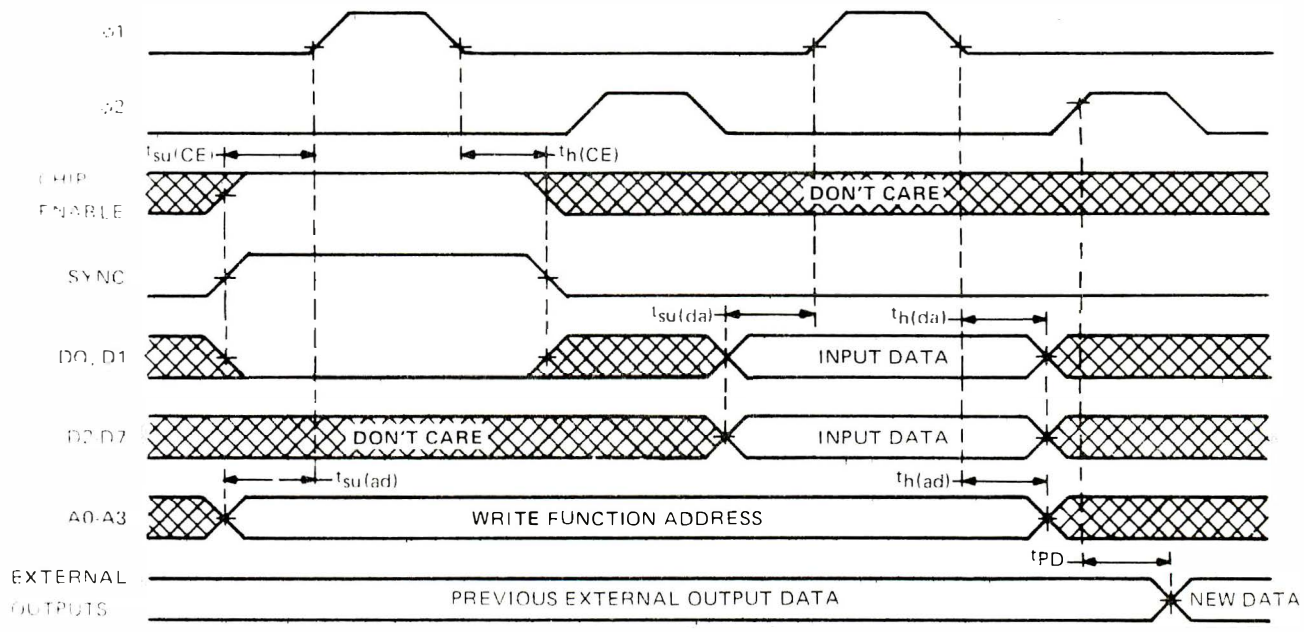
C_L includes probe and jig capacitance

LOAD CIRCUIT



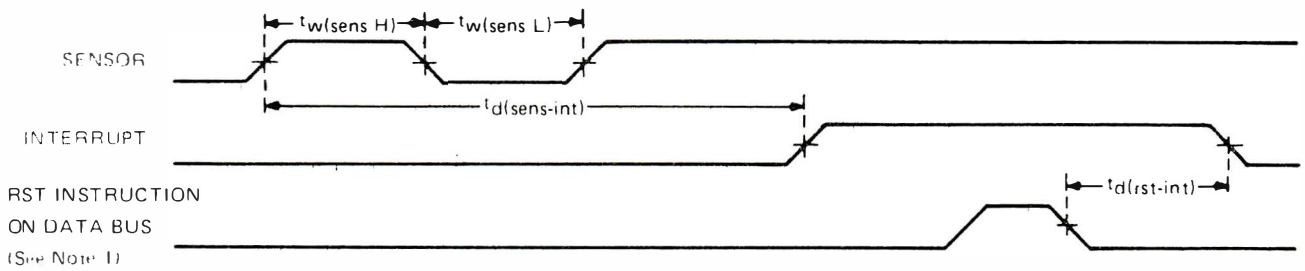
NOTE: For φ1 or φ2 inputs, high and low timing points are 90% and 10% of $V_{IH(\phi)}$. All other timing points are the 50% level.

FIGURE 6–READ CYCLE TIMING



NOTE: For φ1 and φ2 inputs, high and low timing points are 90% and 10% of $V_{IH(\phi)}$. All other timing points are the 50% level.

FIGURE 7–WRITE CYCLE TIMING



NOTES: 1. The RST instruction occurs during the output data valid time of the read cycle.
2. All timing points are 50% of V_{IH}.

FIGURE 8–SENSOR/INTERRUPT TIMING

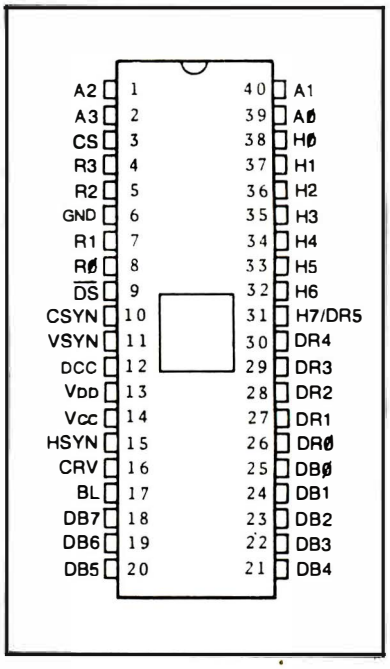
APPENDIX C
5027 CRT CONTROLLER

CRT Video Timer-Controller VTAC

FEATURES

- ☐ Fully Programmable Display Format
  - Characters per data row
  - Data rows per frame
  - Raster scans per data row
  - Raster scans per frame
- ☐ Fully Programmable Monitor Format
  - Horizontal Sync
  - Vertical Sync
  - Composite Sync
- ☐ Programmed via:
  - Processor data bus
  - External PROM
  - Mask option ROM
- ☐ Standard or Non-Standard CRT Monitor Compatible
- ☐ Scrolling
- ☐ Generation of Cursor Video
- ☐ Interlaced and Non-interlaced Operation
- ☐ Vertical Data Positioning
- ☐ TTL Compatibility
- ☐ High Speed Operation
- ☐ COPLAMOS® N-Channel Silicon Gate Technology

PIN CONFIGURATION



General Description

The CRT Video Timer-Controller Chip (VTAC) is a user programmable 40-pin COPLAMOS® n channel MOS/LSI device containing the logic functions required to generate all the timing signals for the presentation and formatting of interlaced and non-interlaced video data on a standard or non-standard CRT monitor.

With the exception of the dot counter, which may be clocked at a video frequency above 25 MHz and therefore not recommended for MOS implementation, all frame formatting, such as horizontal, vertical, and composite sync, characters per data row, data rows per frame, and raster scans per data row and per frame are totally user programmable. The data row counter has been designed to facilitate scrolling.

Programming is effected by loading seven 8 bit control registers directly off an 8 bit bidirectional data bus. Four register address lines and a chip select line provide complete microprocessor compatibility for program controlled set up. The device can be "self loaded" via an external PROM tied on the data bus as described in the OPERATION section. Formatting can also be programmed by a single mask option.

In addition to the seven control registers two additional registers are provided to store the cursor character and data row addresses for generation of the cursor video signal. The contents of these two registers can also be read out onto the bus for update by the program.

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... 0°C to + 70°C
Storage Temperature Range ..... −55°C to +150°C
Lead Temperature (soldering, 10 sec.) ..... +325°C
Positive Voltage on any Pin, with respect to ground ..... +18.0V
Negative Voltage on any Pin, with respect to ground ..... −0.3V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

ELECTRICAL CHARACTERISTICS (T_A= 0°C to 70°C, V_{CC}= +5V ±5%, V_{DD}= +12V ±5%, unless otherwise noted)

Parameter	Min.	Typ.	Max.	Unit	Comments
D.C. CHARACTERISTICS					
INPUT VOLTAGE LEVELS					
Low Level, V_{IL}			0.8	V	
High Level, V_{IH}	V_{CC}−1.5		V_{CC}	V	
OUTPUT VOLTAGE LEVELS					
Low Level—V_{OL} for RØ-3			0.4	V	I_{OL} = 3.2ma
Low Level—V_{OL} all others			0.4	V	I_{OL} = 1.6ma
High Level—V_{OH} for RØ-3	2.4				I_{OH} = 80μa
High Level—V_{OH} all others	2.4				I_{OH} = 40μa
INPUT CURRENT					
Low Level, I_{IL}					
High Level, I_{IH}					
INPUT CAPACITANCE					
Data Bus, C_{IN}				pf	
Clock, C_{IN}				pf	
All other, C_{IN}				pf	
DATA BUS LEAKAGE in INPUT MODE					
I_{DB}					
I_{DB}					
POWER SUPPLY CURRENT					
I_{CC}				ma	
I_{DD}				ma	
A.C. CHARACTERISTICS					T_A = 25°C
DOT COUNTER CARRY					
frequency	0.2	4.0		MHz	Figure 1
PW_H	35			ns	Figure 1
PW_L	190			ns	Figure 1
t_r, t_f		10		ns	Figure 1
DATA STROBE					
$PW_{\overline{DS}}$		150		ns	Figure 2
ADDRESS, CHIP SELECT					
Set-up time		100		ns	Figure 2
Hold time		50		ns	Figure 2
DATA BUS—LOADING					
Set-up time		100		ns	Figure 2
Hold time		75		ns	Figure 2
DATA BUS—READING					
T_{DEL2}		100		ns	Figure 2, CL = 50pf
OUTPUTS: HØ-7, HS, VS, BL, CRV,					
CS-T_{DEL1}		100		ns	Figure 1, CL = 20pf
OUTPUTS: RØ-3, DRØ-5					
T_{DEL3}		1.0		μs	Figure 3, CL = 20pf

Restrictions

1. Only one pin is available for strobing data into the device via the data bus. The cursor X and Y coordinates are therefore loaded into the chip by presenting one set of addresses and outputed by presenting a different set of addresses. Therefore the standard WRITE and READ control signals from most microprocessors must be "NORed" externally to present a single strobe ($\overline{DS}$) signal to the device.

2. An even number of scan lines per character row must be programmed in interlace mode. This is again due to pin count limitations which require that the least significant bit of the scan counter serve as the odd/even field indicator.

3. In interlaced mode the total number of character slots assigned to the horizontal scan must be even to insure that vertical sync occurs precisely between horizontal sync pulses.

Operation

The design philosophy employed was to allow the device to interface effectively with either a microprocessor based or hardwire logic system. The device is programmed by the user in one of two ways; via the processor data bus as part of the system initialization routine, or during power up via a PROM tied on the data bus and addressed directly by the Row Select outputs of the chip. (See figure 4). Seven 8 bit words are required to fully program the chip. Bit assignments for these words are shown in Table 1. The information contained in these seven words consists of the following:

Horizontal Formatting:

Characters/Data Row	A 3 bit code providing 8 mask programmable character lengths from 20 to 132. The standard device will be masked for the following character lengths; 20, 32, 40, 64, 72, 80, 96, and 132.
Horizontal Sync Delay	3 bits assigned providing up to 8 character times for generation of "front porch".
Horizontal Sync Width	4 bits assigned providing up to 16 character times for generation of horizontal sync width.
Horizontal Line Count	8 bits assigned providing up to 256 character times for total horizontal formatting.
Skew Bits	A 2 bit code providing from a 0 to 2 character skew between the horizontal address counter and the horizontal blank and sync signals to allow for retiming of video data prior to generation of composite video signal. The Cursor Video signal is also skewed as a function of this code.

Vertical Formatting:

Interlaced/Non-interlaced	This bit provides for data presentation with odd/even field formatting for interlaced systems. It modifies the vertical timing counters as described below.
Scans/Frame	8 bits assigned, defined according to the following equations: Let X = value of 8 assigned bits. 1) in interlaced mode—scans/frame = 2X + 513. Therefore for 525 scans, program X = 6 (00000110). Vertical sync will occur precisely every 262.5 scans, thereby producing two interlaced fields. Range = 513 to 1023 scans/frame, odd counts only. 2) in non-interlaced mode—scans/frame = 2X + 256. Therefore for 262 scans, program X = 3 (00000011). Range = 256 to 766 scans/frame, even counts only. In either mode, vertical sync width is fixed at three horizontal scans (≡ 3H).
Vertical Data Start	8 bits assigned providing scan line resolution in vertical data positioning with respect to vertical sync. The Data Row Counter is reset at vertical sync and will not begin counting until the scan line selected by these eight bits.
Data Rows/Frame	6 bits assigned providing up to 64 data rows per frame.
Last Data Row	6 bits to allow up or down scrolling via a preload defining the count of the last displayed data row.
Scans/Data Row	4 bits assigned providing up to 16 scan lines per data row.

Additional Features

Device Initialization:

Under microprocessor control—The device can be reset under system or program control by presenting a Ø1Ø1 address on AØ-3. The device will remain reset at the top of the even field page until a start command is executed by presenting a Ø111 address on AØ-3.

Via "Self Loading"—In a non-processor environment, the self loading sequence is effected by presenting and holding the 1111 address on AØ-3, and is initiated by the receipt of the strobe pulse ($\overline{DS}$). The 1111 address should be maintained long enough to insure that all seven registers have been loaded (in most applications under one millisecond). The timing sequence will begin one line scan after the 1111 address is removed. In processor based systems, self loading is initiated by presenting the 111Ø address to the device. Self loading is terminated by presenting the start command to the device which also initiates the timing chain.

Scrolling—In addition to the Register 6 storage of the last displayed data row a "scroll" command (address 11Ø1) presented to the device will increment the first displayed data row count to facilitate up scrolling in certain applications.

Description of Pin Functions

Pin No.	Symbol	Name	Input/ Output	Function
25-18	DBØ-7	Data Bus	I/O	Data bus. Input bus for control words from microprocessor or PROM. Bidirectional bus for cursor address.
3	CS	Chip Select	I	Signals chip that it is being addressed
39,40,1,2	AØ-3	Register Address	I	Register address bits for selecting one of seven control registers or either of the cursor address registers
9	$\overline{DS}$	Data Strobe	I	Strobes DBØ-7 into the appropriate register or outputs the cursor character address or cursor line address onto the data bus
12	DCC	DOT Counter Carry	I	Carry from off chip dot counter establishing basic character clock rate.
38-32	HØ-6	Character Counter Outputs	O	Character counter outputs.
7, 5, 4	R1-3	Scan Counter Outputs	O	Three most significant bits of the Scan Counter; row select inputs to character generator.
31	H7/DR5	H7/DR5	O	Pin definition is user programmable. Output is MSB of Character Counter if MSB of Characters/Data Row word is a "1", otherwise output is MSB of Data Row Counter
8	RØ	Scan Counter LSB (Odd/Even Field)	O	Least significant bit of the scan counter. In interlaced mode this bit defines the odd or even field. In this way, odd scan lines of the character font are selected during the odd field and even scans during the even field.
26-30	DRØ-4	Data Row Counter Outputs	O	Data Row counter outputs.
17	BL	Blank	O	Defines non active portion of horizontal and vertical scans.
15	HSYN	Horizontal Sync	O	Initiates horizontal retrace.
11	VSYN	Vertical Sync	O	Initiates vertical retrace.
10	CSYN	Composite Sync	O	Active in non-interlaced mode only. Provides a true RS-170 composite sync waveform.
16	CRV	Cursor Video	O	Defines cursor location in data field.
14	V_{CC}	Power Supply	PS	+5 volt Power Supply
13	V_{DD}	Power Supply	PS	+12 volt Power Supply

Timing Diagrams

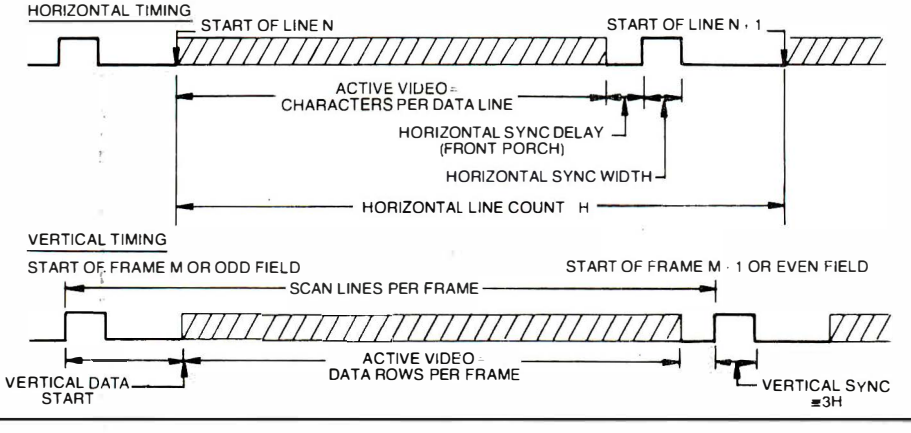
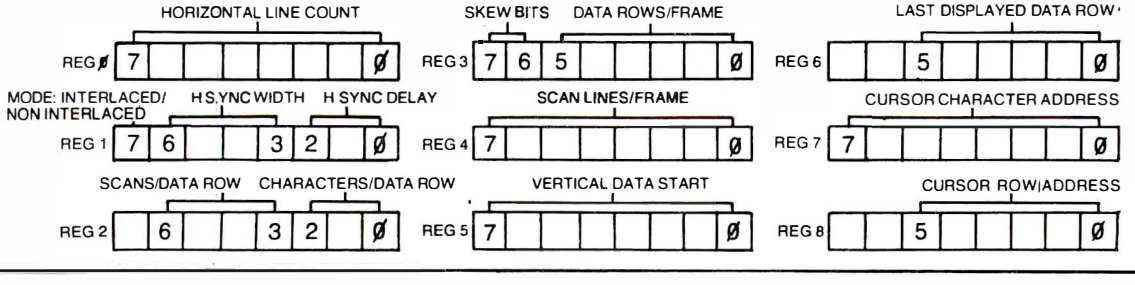


TABLE 1

BIT ASSIGNMENT CHART



Register Selects/Command Codes

A3	A2	A1	AØ	Select/Command	Description
0	0	0	0	Load Control Register Ø	See Table 1
0	0	0	1	Load Control Register 1	
0	0	1	0	Load Control Register 2	
0	0	1	1	Load Control Register 3	
0	1	0	0	Load Control Register 4	
0	1	0	1	Load Control Register 5	
0	1	1	0	Load Control Register 6	
0	1	1	1	Processor Self Load	Command from processor instructing CRT 5027 to enter Self Load Mode
1	0	0	0	Read Cursor Character Address	
1	0	0	1	Read Cursor Line Address	
1	0	1	0	Reset	Resets timing chain to top left of page. Reset is latched on chip by $\overline{DS}$ and counters are held until released by start command.
1	0	1	1	Up Scroll	Increments address of first displayed data row on page. ie; prior to receipt of scroll command—top line = 0, bottom line = 23. After receipt of Scroll Command—top line = 1, bottom line = 0.
1	1	0	0	Load Cursor Character Address	
1	1	0	1	Load Cursor Line Address	
1	1	1	0	Start Timing Chain	Receipt of this command after a Reset or Processor Self Load command will release the timing chain approximately one scan line later. In applications requiring synchronous operation of more than one CRT 5027 the dot counter carry should be held low during the $\overline{DS}$ for this command.
1	1	1	1	Non-Processor Self Load	Device will begin self load via PROM when $\overline{DS}$ goes low. The 1111 command should be maintained on AØ-3 long enough to guarantee self load. (Scan counter should cycle through at least once). Self load is automatically terminated and timing chain initiated when the all "1's" condition is removed, independent of $\overline{DS}$. For synchronous operation of more than one CRT 5027, the Dot Counter Carry should be held low when this command is removed.

NOTE: During Self Load, the scan counter states corresponding to the nine load command addresses will load the appropriate register. Therefore if reseting of the cursor X and Y position registers is required via self load the PROM words for address 11ØØ and 11Ø1 should be programmed as all zeros.

AC TIMING DIAGRAMS

FIGURE 1 VIDEO TIMING

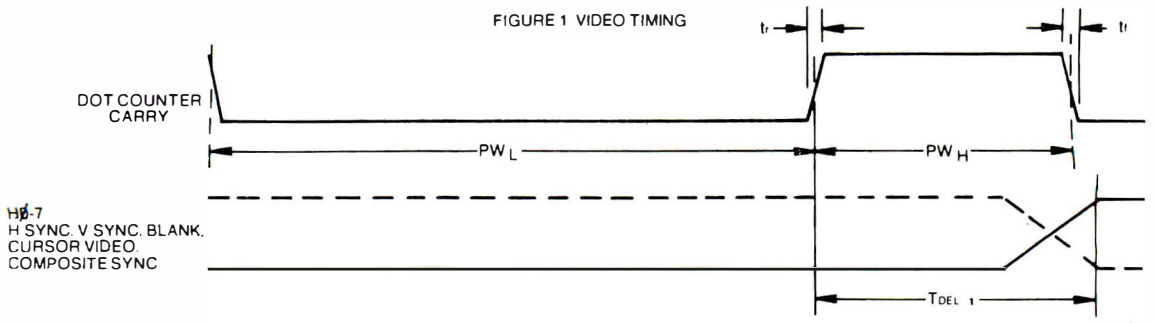


FIGURE 2 LOAD/READ TIMING

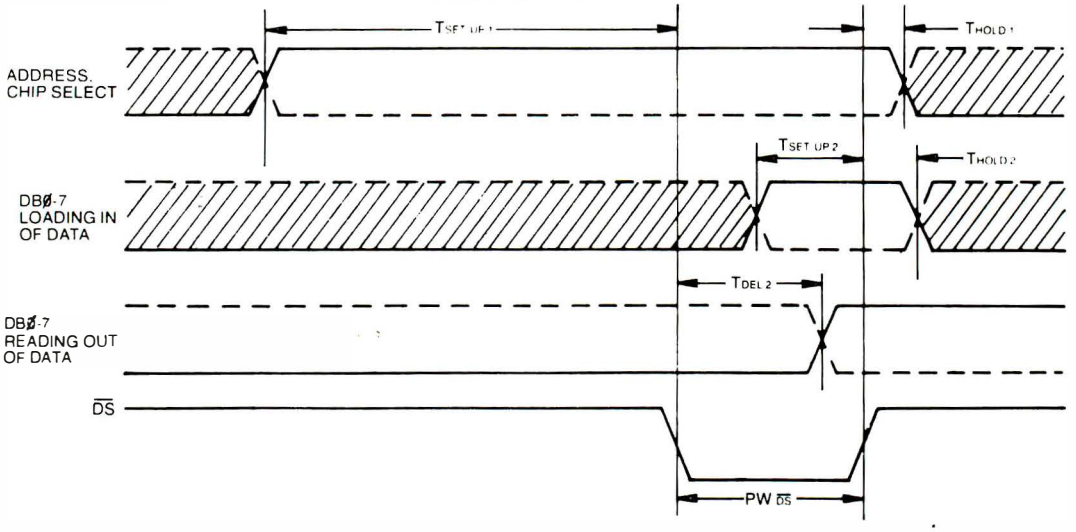


FIGURE 3 SCAN AND DATA ROW COUNTER TIMING

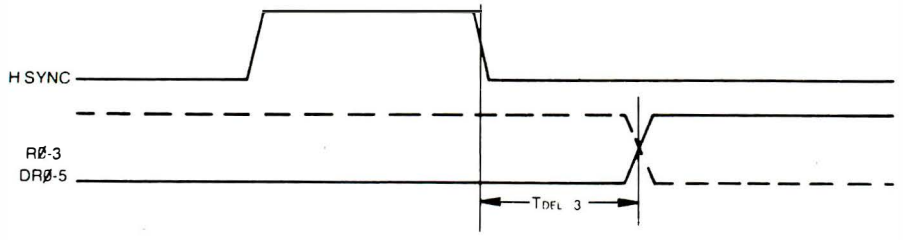
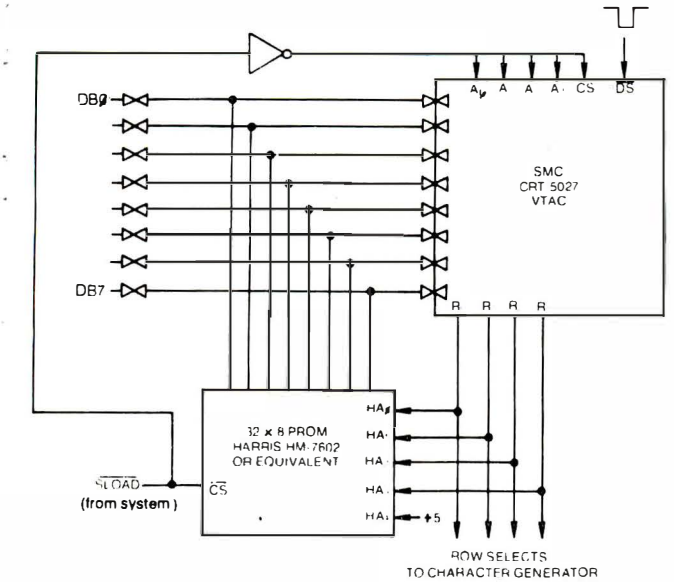
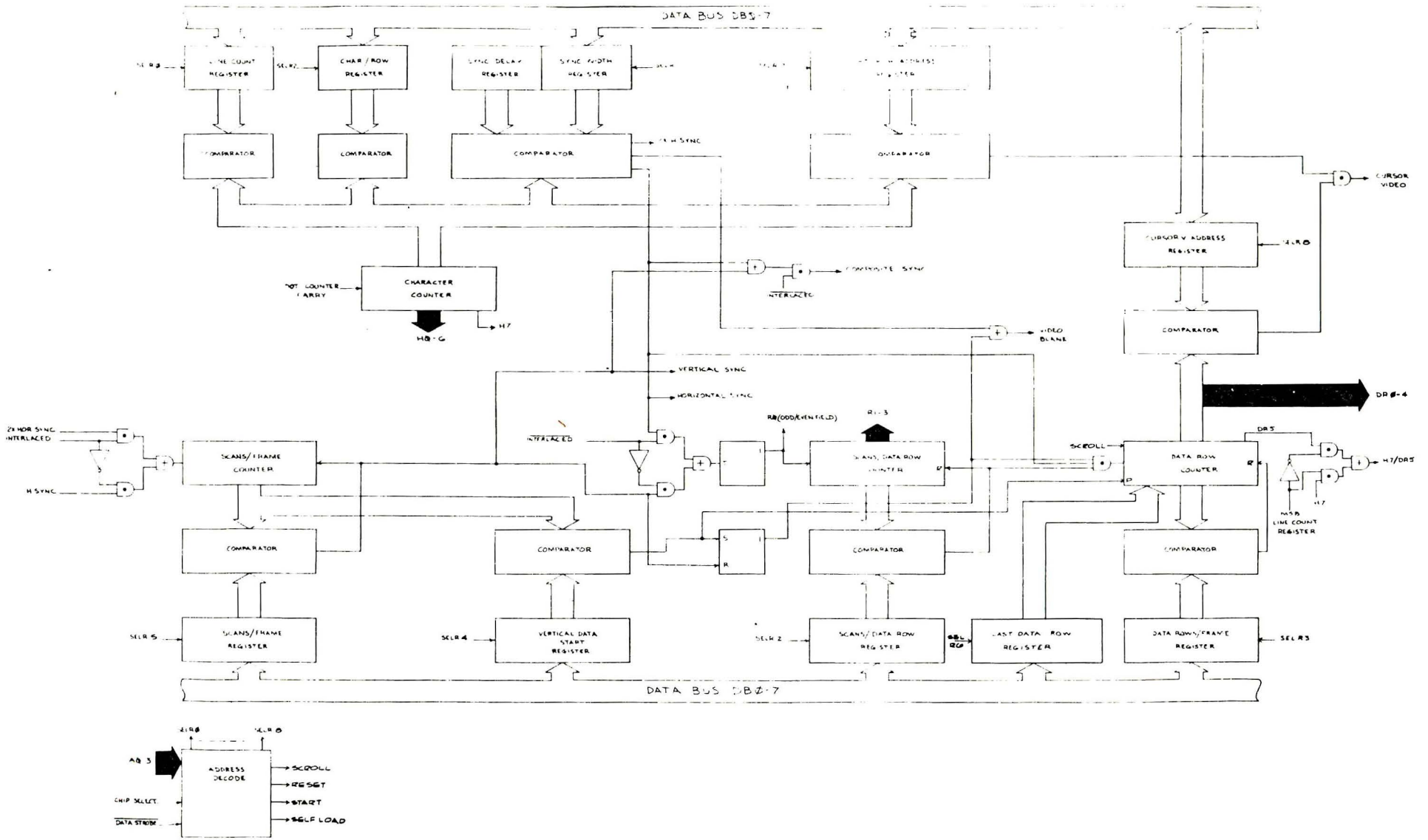


Figure 4. SELF LOADING SCHEME FOR CRT 5027 SET-UP





BLOCK DIAGRAM