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VIDEO-1 by S. Rines

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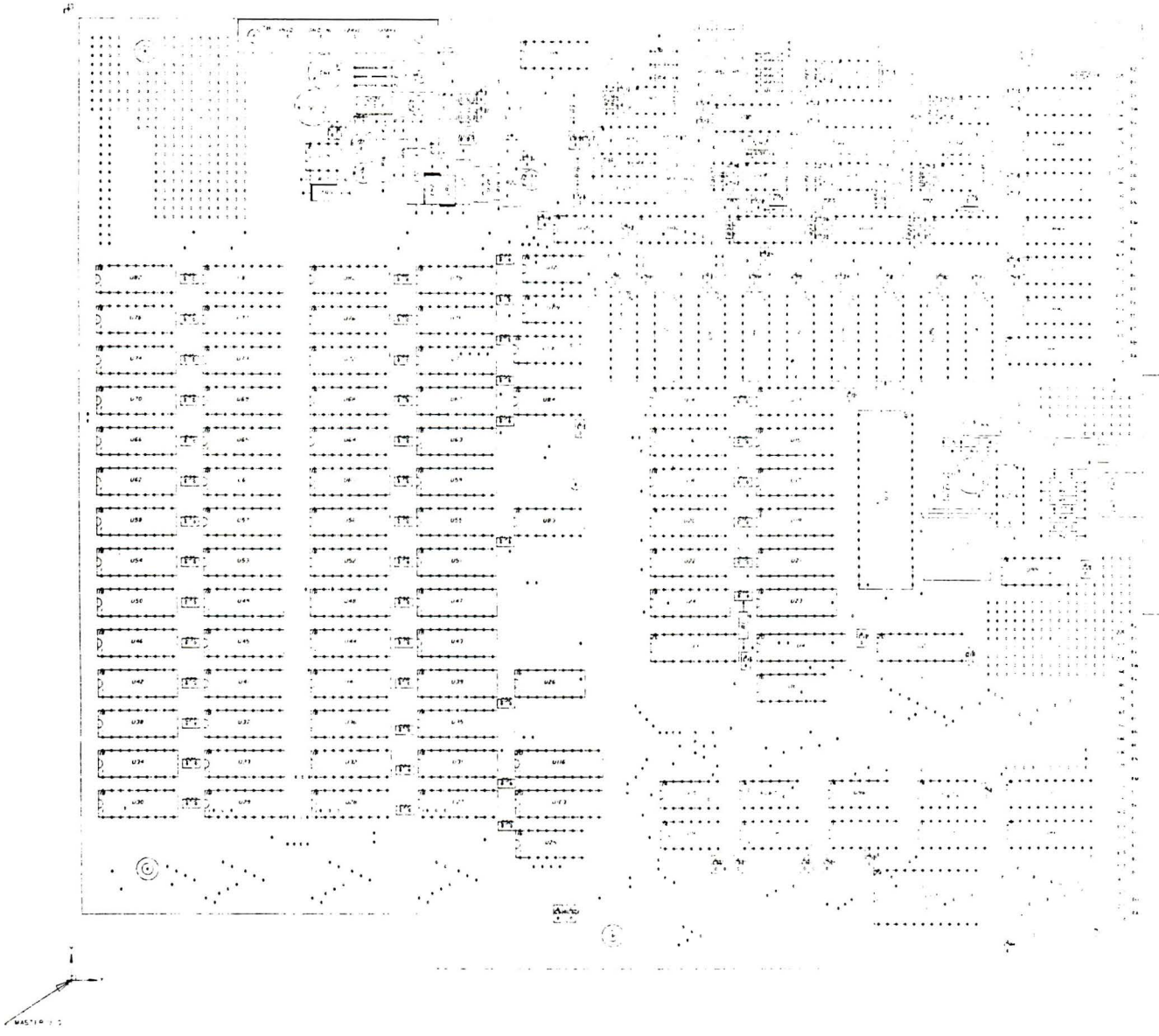


Figure 1-1. VIDEO-1.

1.1 GENERAL

The VIDEO-1 circuit board has been designed to provide users of personal or hobbyist computers with a variety of additional functions not normally provided with their computers. The VIDEO-1 was developed specifically for use with the Rockwell AIM-65, and this manual has been written around the AIM-65's architecture and firmware. Users of other computers will find that the interconnects necessary for VIDEO-1 use are, in most cases, already available on their computer's expansion bus.

The functions provided by the VIDEO-1 are summarized below:

1. Eleven modes of video display (with either RF or video output) which include alphanumerics and either two-color high-density graphics or up to eight-color graphics.
2. Space for 28K of auxiliary static memory.
3. The memory space allocated to video use (6K) may also be utilized as auxiliary memory for a total of 34K.
4. Space for one 2716 EPROM (2K).
5. Sixteen analog outputs from two digital-to-analog converters (eight unipolar outputs and eight bipolar outputs) with up to 65,536 discrete steps.
6. Eight analog inputs to an 8-bit analog-to-digital converter with programmable gain/attenuation and offset.
7. A light pen, capable of operating in any of the eleven video modes.

Each of the above functions has been designed to operate independently of the others (with the exception of light pen dependence on video) to allow maximum flexibility in assembly or operation by the user. Several kits are available to minimize the cost of any given function to the user.

All connections necessary for coupling any function on the VIDEO-1 to the AIM-65 (or other computer) are accomplished via a 40-conductor ribbon cable from VIDEO-1 edge connector J3 to the AIM-65 expansion connector J3 (or the appropriate expansion connector on most other computers).

Edge connector J1 on the VIDEO-1 provides contacts for all analog inputs and outputs and light pen through a standard 44-pin connector.

Connector J2 is a standard RCA phono jack. The output of J2 may be either RF, for application to the VHF antenna terminals of a standard television, or composite video, for use with video monitors, dependent on component selection. (See assembly section.)

The VIDEO-1 circuit board size and shape were established to allow the VIDEO-1 to fit beneath the AIM-65 in any of the various cases currently available from Rockwell or AIM-65 user's groups. (See the outline and mounting drawing for specific dimensions.)

A portion of the VIDEO-1 circuit board has been intentionally left devoid of components. The section has numerous plated-through holes on 0.100-inch centers to facilitate the addition of user-designed circuits or modifications.

1.2 SPECIFICATIONS

The following specifications represent the maximum capabilities of the VIDEO-1. Refer to the operation section for additional information on the requirements necessary to attain the maximum ratings.

Power requirements ..... +5 V dc ±0.2 V @ 6 A.
+24 V dc ±4 V @ 1 A.

Note

Typical power requirements, using standard power 2114 RAM, are about 3.5 A of +5 V dc and 0.7 A of +24 V dc.

Auxiliary memory space ..... 34K bytes (including 6K video memory).

EPROM space ..... 2 kilobytes.

Video

- Alphanumeric format ..... Sixteen lines of 32 characters.
- Color graphics ..... Eight colors.
- Graphics resolution ..... 49,152 controllable elements (with 6K of video memory).

Digital-to-analog converters

- Unipolar outputs ..... Eight 256-bit resolution in 10-mV steps from 0 to 2.56 V.
- Bipolar outputs ..... Eight 65,536-bit resolution in 78-μV steps (with external power supplies) from -2.5 to +2.5 V.

Analog-to-digital converters

- Number of inputs ..... 8.
- Number of steps gain/attenuation ..... 8.
- Number of steps of offset ..... 65,536 (with external power supplies).
- Resolution ..... 8 bits (256 steps).

Light pen resolution ..... 6,144 screen elements definable.

This section describes the general operating procedures for a fully populated VIDEO-1. Operation of the VIDEO-1 with monitor software is described separately in the software section.

2.1 VIDEO

The only power required for video operation is +5 V dc. The video-allocated memory resides at locations 8000_{16} to $97FF_{16}$. A minimum of 1K of memory is required starting at location 8000_{16} for alphanumerics, semigraphics, and the first modes of black-and-white and color graphics. The remainder of the memory allocated for video (from 8400_{16} to $97FF_{16}$) may be added in 1K increments to add graphics density. Refer to table 2-1 for a description of the various modes, mode formats, and memory requirements.

The AIM-65 uses and recognizes only upper-case letters in a 6-bit ASCII format. The VIDEO-1 uses an MC6847 video display generator which also utilizes a 6-bit ASCII format in the alphanumerics modes. Since an 8-bit byte is used for each character, there are two unused bits (D6 and D7). Bit D6 remains unused, but D7 is used to determine whether a given character should be inverted or not. If bit D7 is a logic 1, the character will be inverted.

When the AIM-65 and VIDEO-1 are initially powered up, the video will come up in the maximum graphics mode. Refer to table 2-1 for the data to be written to address $9FFF_{16}$ (the video mode latches) to enable each of the various modes.

The vertical retrace synchronization pulse from the video display generator is connected to bit 0 of the interrupt buffer which occupies memory location $9FF8_{16}$. By inputting data to video memory only while bit 0 of address $9FF8_{16}$ is high, a snow-free display will be maintained.

Refer to the applications ideas section for specific programs for BASIC plotting, graphing, word processing, etc.

2.2 LIGHT PEN

The light pen is used to specify any given screen location by contacting the TV or monitor screen at the intended location. When the electron beam passes the screen location where the pen is being held, a pulse is generated which latches the address of that location into the light pen latches located at memory locations $9FFD_{16}$ (MSbyte) and $9FFE_{16}$ (LSbyte). The acquisition of a light pen address also sets bit 1 of the interrupt buffer located at $9FF8_{16}$. By sampling the data at location $9FF8_{16}$ looking for a logic 1 in bit 1, a jump to a light pen subroutine can be initiated. When reading the address from the light pen, latched address $9FFD_{16}$ must be read first, as the reading of address location $9FFE_{16}$ automatically resets the light pen and enables it to acquire another address.

In order to use the light pen, +24 V dc must be applied to the VIDEO-1 in addition to +5 V dc.

Table 2-1. AIM VIDEO-1 Modes.

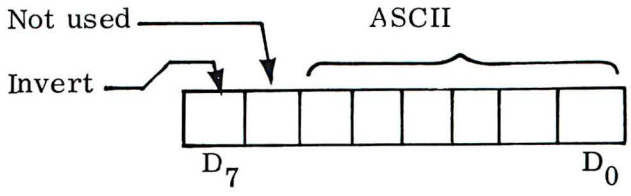
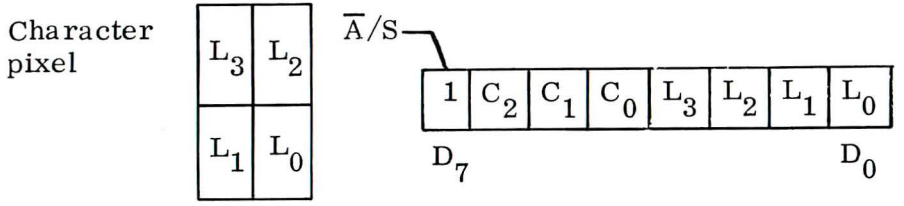
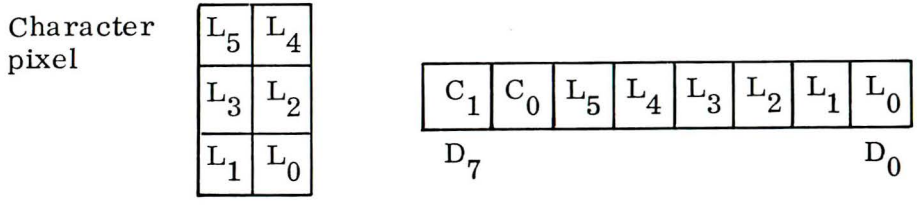
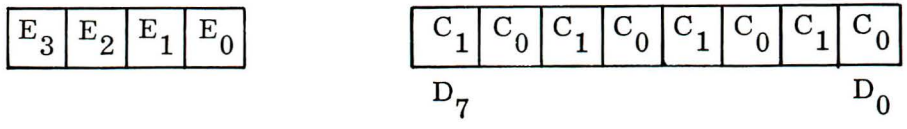
MODE	POKE (40959)/ STA 9FFF	FORMAT	MEMORY REQUIRED
1A, alphanumerics	00, 08/00, 08	512 characters - 32 char/16 lines, 2 sets of 2 colors 	0.5K
1B, semigraphics 4	64, 72/40, 48	2048 elements - 64 across/32 down, 8 colors 	0.5K
1C, semigraphics 6	96, 104/60, 68	3072 elements - 64 across/48 down, 2 sets of 4 colors 	0.5K
2A, color graphics	16, 24/10, 18	4096 elements - 64 across/64 down, 2 sets of 4 colors 	1.0K

Table 2-1. AIM VIDEO-1 Modes (Cont).

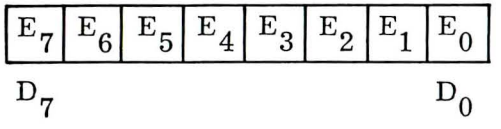
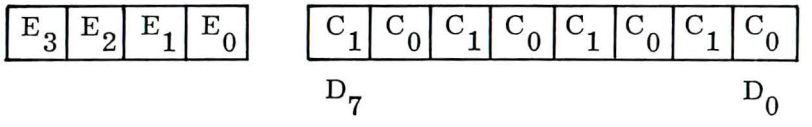
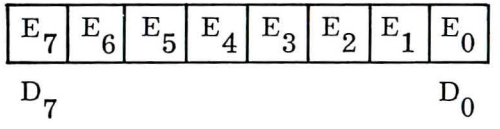
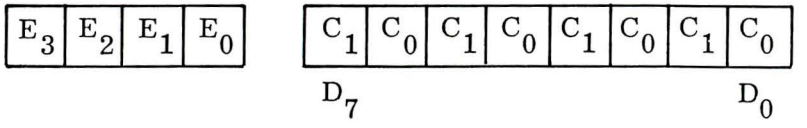
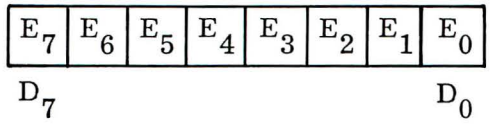
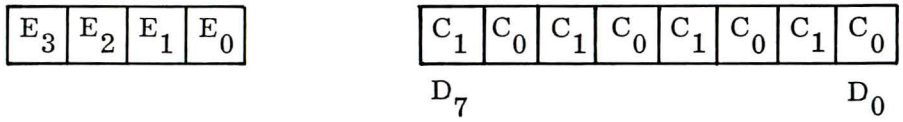
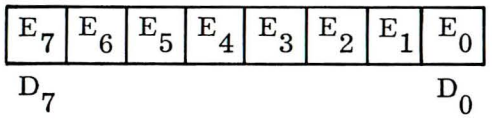
MODE	POKE (40959)/ STA 9FFF	FORMAT	MEMORY REQUIRED
2B, graphics	17, 25/11, 19	8192 elements - 128 across/64 down, 2 sets of 2 colors 	1.0K
3A, color graphics	18, 26/12, 1A	8192 elements - 128 across/64 down, 2 sets of 4 colors 	2.0K
3B, graphics	19, 27/13, 1B	12,288 elements - 128 across/96 down, 2 sets of 2 colors 	1.5K
4A, color graphics	20, 28/14, 1C	12,288 elements - 128 across/96 down, 2 sets of 4 colors 	3.0K

Table 2-1. AIM VIDEO-1 Modes (Cont).

MODE	POKE (40959)/ STA 9FFF	FORMAT	MEMORY REQUIRED
4B, graphics	21, 29/15, 1D	24,576 elements - 128 across/192 down 	3.0K
5A, color graphics	22, 30/16, 1E	24,576 elements - 128 across/192 down, 2 sets of 4 colors 	6.0K
5B, graphics	23, 31/17, 1F	49,152 elements - 256 across/192 down 	6.0K

2.3 AUXILIARY MEMORY

The auxiliary memory decoding circuitry on the VIDEO-1 provides the necessary chip selects for 28K of additional memory that will occupy memory addresses 1000_{16} through $7FFF_{16}$. The physical location of the sockets for any particular address may be determined by using the chart of RAM/EPROM addresses and locations (table 2-2) in conjunction with the Auxiliary Memory Layout Drawing.

If only memory expansion is intended, memory IC's should be installed in sequence starting with address 1000_{16}.

Table 2-2. RAM/EPROM Addresses and Locations.

ADDRESS			RAM LOCATIONS
DECIMAL	HEXADECIMAL		
4096 - 5119	1000 - 13FF		U27, U29
5120 - 6143	1400 - 17FF		U28, U30
6144 - 7167	1800 - 1BFF		U31, U32
7168 - 8191	1C00 - 1FFF		U33, U34
8192 - 9215	2000 - 23FF		U35, U36
9216 - 10239	2400 - 27FF		U37, U38
10240 - 11263	2800 - 2BFF		U39, U40
11264 - 12287	2C00 - 2FFF		U41, U42
12288 - 13311	3000 - 33FF		U43, U44
13312 - 14335	3400 - 37FF		U45, U46
14336 - 15359	3800 - 3BFF		U47, U48
15360 - 16383	3C00 - 3FFF		U49, U50
16384 - 17407	4000 - 43FF		U51, U52
17408 - 18431	4400 - 47FF		U53, U54
18432 - 19455	4800 - 4BFF		U55, U56
19456 - 20479	4C00 - 4FFF		U57, U58
20480 - 21503	5000 - 53FF		U59, U60
21504 - 22527	5400 - 57FF		U61, U62
22528 - 23551	5800 - 5BFF		U63, U64
23552 - 24575	5C00 - 5FFF		U65, U66
24576 - 25599	6000 - 63FF		U67, U68
25600 - 26623	6400 - 67FF		U69, U70
26624 - 27647	6800 - 6BFF		U71, U72
27648 - 28671	6C00 - 6FFF		U73, U74
28672 - 29695	7000 - 73FF		U75, U76
29696 - 30719	7400 - 77FF		U77, U78
30720 - 31743	7800 - 7BFF		U79, U80
31744 - 32767	7C00 - 7FFF		U81, U82
32768 - 33791	8000 - 83FF		U13, U14
33792 - 34815	8400 - 87FF		U15, U16
34816 - 35839	8800 - 8BFF	Video	U17, U18
35840 - 36863	8C00 - 8FFF	RAM	U19, U20
36864 - 37887	9000 - 93FF		U21, U22
37888 - 38911	9400 - 97FF		U23, U24
38912 - 40951	9800 - 9FF7		EPROM location U112

2.4 EPROM

Space and decoding have been provided on the VIDEO-1 for one 2716 erasable programmable read-only memory (EPROM). The EPROM resides at memory locations 9800_{16} through $9FF7_{16}$.

The current configuration allows only reading from the 2716. Monitor software will soon be available in preprogrammed EPROM's for either alphanumerics or graphics operation. Software listings of both monitors have been included as appendix VIII for those individuals wishing to store the programs on tape or blow their own EPROM's.

Refer to the applications ideas section for information on additional circuitry required to write to the VIDEO-1 mounted EPROM.

2.5 DIGITAL-TO-ANALOG CONVERSION

The VIDEO-1 has two separate digital-to-analog (D/A) converters, each with eight possible outputs under microprocessor control. D/A number 1 is a unipolar circuit which provides an analog output from 0 to 2.55 V dc in 10-mV steps. D/A number 2 is a bipolar circuit which provides an analog output from -2.50 to +2.50 V dc in 20-mV steps.

In addition, the output of D/A no. 1 may be utilized as a reference voltage for D/A no. 2 to provide eight possible outputs with 65,536 individual analog steps.

Note

The power supply and digital noise present on the VIDEO-1 will mask the last few bits when utilizing this maximum resolution D/A circuit, limiting the actual resolution to something less than 65,536 discrete steps. While this is perfectly acceptable for most applications, if the VIDEO-1 is to be utilized for laboratory precision waveform generation, off-board power supplies are recommended for the D/A circuitry.

D/A no. 1 resides at memory location $9FFA_{16}$. D/A no. 2 resides at memory location $9FFB_{16}$. Memory location $9FF9_{16}$ is the D/A output latches that control which outputs are enabled and whether D/A no. 1 and no. 2 are operating independently or jointly. The control functions of the D/A output latches are outlined below:

D0, D1, D2 — The D0, D1, and D2 outputs control the D/A no. 1 output demultiplexer. The octal number formed by these bits is the number of the output enabled.

D4, D5, D6 — The D4, D5, and D6 outputs control the D/A no. 2 output demultiplexer. The octal number formed by these bits is the number of the output enabled.

D7 - D7 controls the reference voltage input to D/A no. 2. If D7 is logic 1, D/A no. 2 will operate the same as D/A no. 1 with 256 discrete steps (though bipolar). If D7 is logic 0, the reference voltage input to D/A no. 2 is determined by D3.

D3 - D3 controls the reference voltage input to D/A no. 2 if D7 is logic 0. If D3 is logic 0, the reference voltage for D/A no. 2 is externally controllable by the application of a 0- to +5-V dc level from J1 pin R. If D3 is logic 1, the reference voltage for D/A no. 2 is provided by D/A no. 1.

The D/A output latches need be written only once to specify the appropriate outputs and operating mode. The output waveform(s) are then generated by the data written to either $9FFA_{16}$ (D/A no. 1) or $9FFB_{16}$ (D/A no. 2). Because the data written to either D/A no. 1 or D/A no. 2 is latched, the accuracy of the output waveform is dependent on how often data is written to the latches; a dc level may be generated by merely writing the appropriate data to a D/A converter once.

2.6 ANALOG-TO-DIGITAL CONVERSION

The analog-to-digital (A/D) converter has eight selectable inputs which can be amplified or attenuated under microprocessor control before being converted to an 8-bit digital representation of the input.

Both the A/D input select/gain latches and the A/D converter occupy memory location $9FFC_{16}$. The input select/gain latches accept data from the data bus when $9FFC_{16}$ is written to. The A/D converter provides data to the data bus when $9FFC_{16}$ is read from.

The control functions of the A/D input select/gain latches are as follows:

D4, D5, D6 — The D4, D5, and D6 outputs control which analog input is enabled. The octal number formed by D4, D5, and D6 is the number of the input enabled.

D3 - D3 controls the dc offset applied to the input signal. If D3 is logic 1, no offset is applied. If D3 is logic 0, the dc offset is determined by the output level of D/A no. 2.

D0, D1, D2 — The D0, D1, and D2 outputs control the gain or attenuation of the input signal. (Refer to table 2-3 for the actual gain or attenuation represented by these bits.)

D7 - D7 is not currently used.

Table 2-3. Analog Gains.

D0	D1	D2	OCTAL NUMBER	GAIN APPLIED TO A/D INPUT
0	0	0	0	0.5 (input halved ±10%)
0	0	1	1	1 (unity gain ±10%)
0	1	0	2	2 (±10%)
0	1	1	3	4 (±10%)
1	0	0	4	8 (±10%)
1	0	1	5	16 (±10%)
1	1	0	6	Adjustable (gain of 210 max)
1	1	1	7	Adjustable (for precision unity gain)

Gain no. 6_8 is adjustable to provide the high gain necessary for directly connecting a microphone or other small signal device to the A/D inputs.

To initiate an A/D conversion, read memory location $9FFC_{16}$. When $9FFC_{16}$ is read, the A/D converter initiates a conversion. Nine microseconds later, the conversion is complete. A second reading of $9FFC_{16}$ provides a valid digital representation of the analog sampled. It should be noted that the second read also initiates another conversion.

2.7 INTERRUPT BUFFERS

The interrupt status buffers located at memory location $9FF8_{16}$ are used by the VIDEO-1 to flag when the video is in vertical retrace (bit 0) or when the light pen has latched (bit 1). The remaining bits (2 through 7) have been routed to edge connector J1. These six inputs may be used for indicating any change of state in an external device providing the inputs conform to a logic 0 of ground and a logic 1 of +5 V dc.

Table 2-4 shows VIDEO-1 J1 connections.

Table 2-4. VIDEO-1 J1 Connections.

J1-1	Interrupt status buffer bit 3	J1-A	Interrupt status buffer bit 2
J1-2	Interrupt status buffer bit 4	J1-B	Interrupt status buffer bit 5
J1-3	Interrupt status buffer bit 6	J1-C	Interrupt status buffer bit 7
J1-4	Logic ground	J1-D	D/A #1 output 4
J1-5	D/A #1 output 2	J1-E	D/A #1 output 6
J1-6	D/A #1 output 1	J1-F	D/A #1 output 0
J1-7	D/A #1 output 7	J1-H	D/A #1 output 5
J1-8	D/A #1 output 3	J1-J	Analog -5 V dc
J1-9	Logic +5 V dc	J1-K	Analog +5 V dc
J1-10	Analog ground	J1-L	D/A #2 output 4
J1-11	D/A #2 output 2	J1-M	D/A #2 output 6
J1-12	D/A #2 output 1	J1-N	D/A #2 output 0
J1-13	D/A #2 output 7	J1-P	D/A #2 output 5
J1-14	D/A #2 output 3	J1-R	D/A #2 gain control
J1-15	A/D input 4	J1-S	A/D input 2
J1-16	A/D input 6	J1-T	A/D input 1
J1-17	A/D input 0	J1-U	A/D input 7
J1-18	A/D input 5	J1-V	A/D input 3
J1-19	A/D input select bit 0	J1-W	A/D input select bit 1
J1-20	A/D input select bit 2	J1-X	A/D serial data out
J1-21	Analog ground	J1-Y	A/D sample pulse
J1-22	Light pen collector (+5 V)	J1-Z	Light pen emitter (input)

3.1 AIM-64 INTERFACE

All communication between the AIM-65 and the VIDEO-1 is done via a user-built interconnect cable connected between connector J3 on the AIM-65 and connector J3 on the VIDEO-1. Refer to the assembly section for specific interconnect cable assembly information.

While the VIDEO-1 does not make use of all the possible connections available from the AIM-65 expansion connector, J3, the connections not used are made available on the VIDEO-1 for use with user-designed circuitry. Refer to the AIM-65 User's Guide, page 7-8, for a listing of the connections possible through the expansion connector.

All voltages required for the VIDEO-1 are generated from +5 V dc and +24 V dc supplied to the VIDEO-1 through terminal block TB1. The on-board power supply provides +15, +8, -8, +5, and -5 V dc to the analog section of the VIDEO-1.

3.2 COMMON BUFFERS, TRANSCEIVERS, AND ADDRESS DECODING

Refer to schematic sheet 4. Address lines A_0-A_{15} from the AIM-65 are applied to 8-bit buffers U85 and U86. The buffered address lines from U85 and U86 are routed to the function decoding circuitry, auxiliary memory decoding, and EPROM U112.

Data lines D_0-D_7 from the AIM-65 are routed to data transceivers U2, U116, and U117 and EPROM U112.

Buffered address lines AB15, AB14, AB13, and AB12 are compared against 0000_2 in 4-bit comparator U5. The A=B output of U5 will be high only if the address currently on the bus is less than $0FFF_{16}$. The A=B output of U5 is NOR'ed with buffered address line AB15 in U98B. If either U5 A=B output or AB15 is high, the output of U98B is low; therefore, the output of U98B can be high only for addresses between 1000_{16} and $7FFF_{16}$, which is the area of memory allocated to memory expansion.

The output of U98B is applied to NAND gate U87D along with the phase-2 clock from the AIM-65. The output of U87D will be low during the positive-going half-cycle of phase 2 if a valid address is present. The output of U87D is applied to auxiliary memory data transceiver U116, pin 19, $\overline{CE}$, to enable data transfer through U116. The direction of data transfer through U116 is controlled by the input on pin 1, DIR, which is connected to the $\overline{R/W}$ line from the AIM-65.

Buffered address lines AB15, AB14, and AB13 and the phase-2 clock are compared against 1100_2 in 4-bit comparator U7. The A=B output of U7 will go high only if the current bus address is between 8000_{16} and $9FFF_{16}$. The memory allocated to video, function circuitry (D to A, A to D, and light pen), and EPROM fall within these addresses.

Buffered address lines AB12, AB11, and AB10 are compared against 110_2 in 4-bit comparator U8. The A<B output of U8 is NAND'ed with the A=B output of U7 in U87B. The output of U87B is low if the current address is between 8000_{16} and $97FF_{16}$. This area of memory

has been allocated to video data storage. The output of U87B is routed to address buffers U3 and U4 and video display generator U12 on schematic sheet 1.

The A=B output of U7 and A<B output of U8 are also NAND'ed in U10A in conjunction with the phase-2 clock. The output of U10A goes to data transceiver U2, pin 19, $\overline{CE}$, to enable data transfer to and from video memory during the period when phase 2 is high. Direction of data transfer through U2 is dependent on the state of the AIM $R/\overline{W}$ line which is applied to pin 1 of U2.

The EPROM U112 is selected by the following sequence: the A=B output of U7 is NAND'ed with A=B output of U8 in U87A, the output of which is low if the current address is between 9800_{16} and $9BFF_{16}$. The A=B output of U7 is also NAND'ed with the A>B output of U8 in U10B. The third input to NAND gate U10B comes from 8-input NAND gate U9. The output of U9 is low if address lines A9, A8, A7, A6, A5, A4, and A3 are simultaneously high. The output of U10B is low if the current address is between $9C00_{16}$ and $9FF7_{16}$. If either input to NAND U113B (from U87C and U10B) is low, the output is high. The output of U113B is inverted by U113A and applied to the $\overline{CE}$ input of EPROM U112 which occupies memory address locations 9800_{16} through $9FF7_{16}$.

The remaining portion of the common decoding enables the digital-to-analog, analog-to-digital, light pen, and mode latch circuits. The A=B output of U7 is NAND'ed with the A>B output of U8 in U87C. The output of U87C (9C00 to 9FFF) is applied to one of the $\overline{ENABLE}$ inputs (G2A, pin 4) of 1-of-8 decoder U118. The other $\overline{ENABLE}$ input of U118 (G2B, pin 5) comes from 8-input NAND U9. The ENABLE input (G1, pin 6) comes from the phase-2 clock. The outputs of U118 are selected by address lines A0, A1, and A2 and specify addresses $9FF8_{16}$ through $9FFF_{16}$. OR and NOR gates U119A, B, C, and D and U120D and B condition the outputs of U118 to be high or low in conjunction with the $R/\overline{W}$ line to satisfy the requirements of each application (ie, read, write, clock, or enable). Refer to the digital-to-analog, analog-to-digital, light pen, or video paragraphs of the theory section for the specific condition of each line from U118, U119, or U120.

3.3 VIDEO CIRCUITRY

Refer to schematic sheet 1. Video is generated on the VIDEO-1 by a video display generator (VDG) in conjunction with an RF modulator. The VDG is a Motorola MC6847; the RF modulator is a Motorola MC1372. Data sheets on both devices are included as appendixes I and II. Appendix IV contains the appropriate timing, sync, levels, and phase difference diagrams for the MC6847, in addition to detailed systems aspects. Appendix V contains information on converting the VIDEO-1 for use with PAL or SECAM television systems.

The video display generator is separated from the AIM-65 by data transceivers and address buffers because the VDG acts like a simple microprocessor, sequentially addressing and reading the memory allocated to it. The VDG takes the data and, depending on the operating mode, either generates characters at specific screen locations or shifts the data out serially (after adding the necessary timing pulses) to the screen for display as graphics.

Data written to or read from the video allocated memory must pass through data transceiver U2. U2 is a tristate device which places a high impedance on both the input and output pins when not enabled, allowing the AIM-65 data bus and the VDG data bus to run simultaneously.

Enable line P3 from the common decoding circuitry is applied to the memory select ($\overline{MS}$) input of VDG U11 and the enable inputs of address buffers U3 and U4. When an address between 8000_{16} and $97FF_{16}$ is present on the AIM-65 address bus, the logic 0 on line P3

will suspend operation of VDG U11, placing U11 data and address pins in a high impedance state. At the same time address buffers U3 and U4 are enabled allowing the AIM-65 access to the memory chips resident on the VIDEO-1 at locations 8000_{16} to $97FF_{16}$ (U13 through U24).

The system R/$\overline{W}$ line from the AIM-65 is also buffered through U3. Pull-up resistor R1 holds the R/$\overline{W}$ output from U3 at a logic 1 at all times that the AIM-65 is not writing to a location within that area of memory allocated to video use.

Either the buffered address lines, A10, A11, and A12 from U4, or the DA10, DA11, and DA12 address lines, from the VDG U11, are decoded by memory select U6. Memory select U6 is a 1-of-10 decoder, but the grounding of input D limits the outputs to 1 of 8. Only six of the eight possible output lines are used to enable the six pairs of 2114 RAM used by the VDG.

Data may be read from or written to the video allocated memory the same as any other portion of memory.

Operation of the VDG is dependent on the mode selected by 8-bit mode latch U1. The outputs of U1 are connected to the VDG and control the following:

BIT			
0	GM0		Graphics mode selects
1	GM1		
2	GM2		
3	CSS	-	Color set select
4	$\overline{A}$/G	-	Alphanumerics/graphics select
5	$\overline{INT}$/EXT	-	In alphanumerics, this input selects either the internal ROM or an external character generator. In semigraphics, this input selects either 4 or 6 divisions of the character pixel.
6	$\overline{A}$/S	-	Alphanumerics/semigraphics
7	--	-	Unassigned

The inputs of U1 are the data lines from function data transceiver U117. Data is clocked into mode latch U1 by writing to address $9FFF_{16}$. The common decoding circuitry provides a low from U118 (when address $9FFF_{16}$ is valid) to NOR gate U120B. The $\overline{R/\overline{W}}$ line is inverted by U10C and provides the other input to U120B. The output of U120B is a logic high pulse the width of the phase-2 positive half when $9FFF_{16}$ is being written to. Gate U120A is used as an inverter to provide a logic low pulse. Mode latch U1 clocks the data on the data bus into its latches on the positive transition of the pulse from U120A.

The inverting control input to the VDG (INV) is tied to data line D7. In the alphanumeric mode, if D7 is logic 1, the character being displayed will be inverted. The inverting input has no effect in the other operating modes. VDG U11 receives its clock from a crystal controlled oscillator within RF modulator U12 through NAND gate U99D. Variable capacitor C6 is used to set the oscillator frequency to 3.579545 MHz for use by the VDG and RF modulator. Duty cycle adjustment potentiometer R8 is used to set the duty cycle of the 3.579545-MHz clock to 50 percent.

The VDG output is applied to the RF modulator on the phase-A, phase-B, luminescence (Y), and chromatic bias lines. The RF modulator mixes these signals and steps up the frequency to that determined by the tank circuit consisting of C2 and L1. Adjustment of L1 sets the RF frequency available at connector J2.

Note

For video output, a diode will be installed in place of C2 and L1. (Refer to figure 4-5.)

The field sync ($\overline{FS}$) output of the VDG is inverted by U99C and applied to the bit-0 input of interrupt status buffer U88. Interrupt status buffer U88 occupies memory address $9FF8_{16}$. Data is read from U88 when the common decoding circuitry provides a logic low to U88 output enable ($\overline{OE}$) from U118.

3.4 LIGHT PEN

Refer to schematic sheet 2. The light pen utilizes the sequential addressing technique of the VDG to locate a given screen location by picking up the television's electron beam as it illuminates a screen dot and by generating a pulse to latch the next sequential address. By subtracting a fixed number from the address in the light pen latches (to allow for propagation and processing delays), the actual location of the light pen can be determined.

The light pen consists of an aluminum tube which houses a Darlington MRD370 phototransistor (Q3) connected by a twisted, shielded pair to pins 22 and Z of VIDEO-1 connector J1. When the electron beam passes the mouth of the light pen tube, the photocell conducts and passes voltage to the inverting input of comparator U89A. The noninverting input has an adjustable threshold to fix the sensitivity of the light pen.

The output of the light pen comparator sets J-K flip-flop U90A which provides the positive transition necessary to clock light pen latches U91 and U92, latching the current VDG address and setting bit 1 of interrupt status buffer U88.

The light pen latches are located at memory address locations $9FFD_{16}$ (MSbyte) and $9FFE_{16}$ (LSbyte) and are enabled by their respective select lines from 1-of-8 decoder U118 in the common decoding circuitry (schematic sheet 4). Address $9FFD_{16}$ must be read first. When address $9FFE_{16}$ is enabled by U118, that enable line is also inverted by U120C and applied to the K-input of flip-flop U90A. The clock input of U90A is fed by phase 2 from the AIM-65, so the Q-output of U90A goes low on the next trailing edge of phase 2 and prepares U90A for the next light pen input.

3.5 EPROM

Refer to schematic sheet 4. Erasable programmable read-only memory (EPROM) U112 occupies memory locations 9800_{16} through $9FF7_{16}$ and provides the space for video system firmware or other user programs. The EPROM chosen for use on the VIDEO-1 is a 2716 which requires only +5 V dc to operate in read-only applications.

If U112's socket is to be used for programming user-generated data, some modifications will be required to enable the user to write to the EPROM. Refer to the applications ideas section for information on programming the U112.

Address decoding for U112 is provided by the common decoding circuitry. A description of its operation is included in the common decoding circuitry description, paragraph 3.2.

3.6 AUXILIARY MEMORY

Refer to schematic sheet 3. Space for up to 28K of auxiliary memory has been provided on the VIDEO-1. Static 2114 memories are used throughout the auxiliary memory. The 2114 IC is a 1K by 4 device; therefore, two 2114's are required for each 1K byte of memory.

Addressing of the auxiliary memory is accomplished using the AIM-65 address bus lines. Address lines A0 to A9 through line buffers U85 and U86 are applied to the A0 to A9 inputs of each 2114 for internal decoding. Address lines A10 to A15 through line buffer U85 are applied to 1-of-8 decoders U25, U26, U83, and U84 to generate the specific chip select enables ($\overline{CS}$) for each pair of 2114's. Refer to table 2-2 for an address-versus-component designator listing for the memory section of the VIDEO-1.

The data bus from the AIM-65 through bus transceiver U116 is applied to all pairs of 2114's, D0-D3 being routed to one 2114 and D4-D7 to the other. The system R/$\overline{W}$ line from the AIM-65 is applied to eight line drivers in U103 in parallel. The eight outputs of U103 provide a buffered R/$\overline{W}$ signal to all 56 locations of the 2114's.

3.7 DIGITAL-TO-ANALOG CONVERSION

Refer to schematic sheet 2. The VIDEO-1 has two digital-to-analog (D/A) converters, each of which feeds a 1-of-8 demultiplexer to provide up to 16 separate analog outputs. The normal resolution of any one output is 256 steps; however, by utilizing the analog output of D/A no. 1 to provide a dc reference voltage to D/A no. 2, up to eight outputs are available with 65,536 discrete steps each. D/A no. 1 outputs are unipolar, while D/A no. 2 outputs are bipolar.

Note

While the circuitry is capable of producing 65,536 discrete analog steps, noise from the various circuits on the VIDEO-1 will somewhat degrade the performance of this stage, and a transition in the lower-order bits may not be measurable.

D/A no. 1 and D/A no. 2 occupy memory locations $9FFA_{16}$ and $9FFB_{16}$ respectively.

When address 9FFA is selected, a low from U118 (pin 13) provides one input to OR gate U119B. The other input of U119B comes from NAND gate U10C which is low if a write operation is occurring. When the output of U119B again goes high (at the trailing edge of phase 2), data from the data bus is latched into 8-bit latch U105. The eight outputs of U105 are constantly enabled and provide the digital inputs to digital-to-analog converter U107.

The output of U107 (pin 4) is a variable current source which is directly proportional to the digital input. Adjustment of the analog step voltage out is accomplished with potentiometer R21. The output of U107 is applied to the inverting input of operational amplifier U109. U109 converts the varying current from U107 to varying voltage for application to 1-of-8 demultiplexer U110. The output of U109 is also applied to analog switch U122 for use as a reference voltage for D/A no. 2.

D/A no. 2 operation is similar to that of D/A no. 1, with the exception that the reference voltage to digital-to-analog converter U108 is selected by the condition of the analog switches within U122. A simplified schematic of D/A no. 2 is shown in figure 3-1.

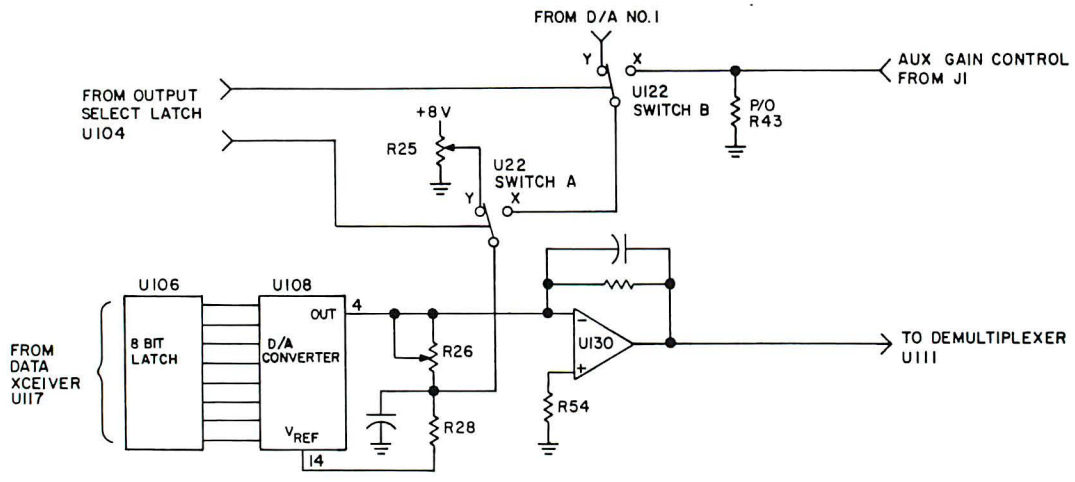


Figure 3-1. D/A No. 2, Simplified Schematic.

A logic 1 from bit 7 of output select latch U104 sets switch A to the position shown in figure 3-1. In this condition, D/A no. 2 would operate the same as the description provided for D/A no. 1, with R25 adjusting the step size.

A logic 0 from U104 to the A-input of U122 switches A to the X-side and enables either D/A no. 1 or an external gain control voltage to provide the reference voltage to U108 determined by the logic level of bit 3 from U104. In this configuration, either the D/A no. 1 output or an external reference voltage sets the voltage level of each analog step. Potentiometer R26 provides an offset cancelling effect by providing an offset to U108 output equal to half the voltage reference. This allows the output of D/A no. 2 to maintain a 0-V reference, while providing an additional 256 steps of resolution to each single step of output.

The output of operational amplifier U130 is routed to 1-of-8 demultiplexer U111 and to switch C of U122 for application to the analog-to-digital converter.

CAUTION

THE AUXILIARY GAIN CONTROL INPUT TO D/A NO. 2 FROM J1, IF USED, MUST BE BETWEEN 0 AND +5 V DC. APPLICATION OF A NEGATIVE VOLTAGE TO THIS INPUT COULD DAMAGE U108.

Output select latch U104 occupies memory location $9FF9_{16}$ and is clocked on the trailing edge of phase 2 when written to. Bits 0-2 of U104 specify the output of demultiplexer U110

for D/A no. 1. Bit 3 controls switch B of U122. Bits 4-6 specify the output of D/A no. 2 through demultiplexer U111, and bit 7 controls switch A of U122.

3.8 ANALOG-TO-DIGITAL CONVERSION

The analog-to-digital (A/D) converter consists of a multiplexer which selects any one of eight inputs, a gain-selectable operational amplifier with selectable dc offset, a comparator, a digital-to-analog converter, and a successive approximation register (SAR).

After software selecting a specific input, specifying the gain or attenuation and dc offset to be applied to the input signal, the A/D compares the input against the output of a D/A converter. The comparator output is used to reset each bit in the successive approximation register (which feeds the D/A) until a null is reached when the D/A output equals the analog input. The byte generated within the SAR is then latched and may be read by the AIM-65.

Input select/gain latch U96 and A/D output latch U102 both occupy memory location $9FFC_{16}$. When address $9FFC_{16}$ is specified, U118 (pin 11) goes low and provides a logic 0 input to NOR gate U120D and OR gate U119D. The other input to U120D is $\overline{R/W}$ from the AIM-65. The output from U120D is high if 9FFC is selected and a read instruction is being executed. The other input to U119D is logic 0 if a write operation is being performed; therefore, the output of U119D is logic 0 if memory location 9FFC is being written to. When the logic 0 from U119D transitions to logic 1 (at the trailing edge of phase 2), data is clocked into U96.

The outputs of U96 control input multiplexer U93 (bits 0-2), dc offset enable (bit 3), and gain select multiplexer U95 (bits 4-6). Bit 7 from U96 is uncommitted.

Analog inputs from the J1 connector are selected by multiplexer U93. The input selected is applied to the noninverting input of operational amplifier U94.

Opamp U94 is configured for unity gain to provide a high input impedance unity gain buffer for the various inputs. The output of U94 through R38 is applied to the inverting input of operational amplifier U131, the feedback loop of which must pass through any one of resistors R46-R51 or potentiometers R52 or R53, as selected by multiplexer U95. The resistor selected by U95 in conjunction with R38 determines the gain or attenuation of opamp U131 and is given by the formula $\frac{\text{Rselected}}{\text{R38}} = \text{gain}$.

Potentiometers R52 and R53 may be set for specific applications by the user. Potentiometer R52 is intended to provide a direct microphone input or other application where precise high gain is required. Potentiometer R53 is intended for precisely setting the A/D circuit to unity gain.

The noninverting input to U131 comes from analog switch C inside U122. If bit 3 from U96 is low, the noninverting input of U131 comes from R37 which sets the nominal voltage offset. If bit 3 from U96 is logic 1, the noninverting input to U131 comes from D/A no. 2, allowing the user to software select the A/D offset voltage.

From U131, the input signal is applied to inverting, unity gain amplifier U97 to reinvert the signal to match the original input's phase before being applied to the plus input of comparator U89B.

The minus input of comparator U89B comes from operational amplifier U124 which provides the current-to-voltage conversion for digital-to-analog converter U101. The maximum voltage from U101 is set by the adjustment of the reference voltage in with potentiometer R31. The digital input to U101 is provided by the successive approximation register, U100.

The successive approximation register (SAR), U100, clocked by $\overline{\text{phase 2}}$ from U121B, sequentially sets or resets each of 8 bits starting with the most significant bit. The output of the SAR through D/A U101 is compared against the input as the SAR sets each bit. For each step, if the SAR's equivalent analog voltage is greater than the input voltage, the active bit is reset.

When memory address $9FFC_{16}$ is read by the AIM-65, the logic 1 from U120D in the common decoding circuitry triggers monostable multivibrator U123 which provides the start pulse to SAR U100. The conversion process occurs automatically after being initiated by the start pulse and requires 8 microseconds from the first leading edge of $\overline{\text{phase 2}}$, which occurs during the start pulse. At the end of the conversion process, the conversion complete ($\overline{\text{CC}}$) signal from SAR U100, pin 2, is inverted by NAND gate U121C. The positive transition from U121C clocks the SAR data into 8-bit latch U102. Another read of address $9FFC_{16}$ transfers the data from U102 to the AIM-65 and initiates another conversion cycle.

Writing to address $9FFC_{16}$ will modify the data in latch U96 but will not initiate a conversion.

The A/D sample pulse may be monitored at J1 connector, pin Y, for custom sample and hold applications.

3.9 POWER SUPPLIES

Refer to schematic sheet 4. The only voltages required by the VIDEO-1 are +5 V dc and +24 V dc.

The +5 V dc provided at TB1 feeds all the digital circuitry on the VIDEO-1 and is labeled +5VDC (L) on the schematics.

The +24 V dc provided at TB1 is used exclusively for the analog circuitry. From TB1, +24 V dc is applied to 3-leg regulator U114 to generate +15 V dc. The +15 V dc from U114 is fed to 3-leg regulators U125, U127, and U128. The output of U125 is +8 V dc, while the outputs of U127 and U128 are both +5 V dc. Two +5-V dc regulators are utilized to isolate the linear circuitry in the digital-to-analog and analog-to-digital sections from the CMOS switches and multiplexers.

The output of U114 is also applied to 555 timer U115. Timer U115 is being utilized in the astable multivibrator mode, the duty cycle of which is determined by the charge time of C70 through R15 and CR3 and the discharge time of C70 through R17 to pin 7. The square-wave output from U115, pin 3, is applied to the bases of Q1 and Q2. When the U115, pin 3, output is high, Q1 is turned on, providing +15 V to the plus side of capacitor C72. Negative charge is drawn from ground through CR2 to the minus side of C72. When the square wave from U115 goes low, Q1 is turned off and Q2 is turned on, allowing the plus side of C72 to discharge to ground. The negative potential on the minus side of C72 is isolated from ground by CR2 and discharges instead through CR1. Coil L2 filters the switching transitions from CR1.

The negative square wave from L2 is filtered by C73 and applied to 3-leg regulators U126 and U129 to provide -8 V dc and -5 V dc, respectively. The -8 V dc provides the negative voltage necessary for the bipolar opamps and also for the internal resistance ladders within the D/A converters. The -5 V dc provides the negative voltage required by the CMOS switches and multiplexers for bipolar operation.

Assembly of the VIDEO-1 should be done in segments with functional testing performed between those segments to simplify fault-finding. This section will provide a recommended assembly sequence and the test procedures for verifying each stage of the assembly.

The following equipment is needed for assembly and test:

1. Equipment Required for Assembling the VIDEO-1

   a. Soldering iron -- 30 watts maximum, with 1/16-inch-wide tip.
   b. Solder -- 60/40, rosin core, 22 gage.
   c. Needle-nose pliers.
   d. Dykes.
   e. Dampened sponge (to clean soldering iron tip).
   f. Solder sucker (just in case).

2. Equipment Required for Assembly Testing

   a. VOM.
   b. AIMS-65 with AIM to VIDEO-1 interconnect cable and power cables.
   c. Oscilloscope, 10 MHz (optional).

4.1 AIM-65/VIDEO-1 POWER CABLES

The VIDEO-1 requires both +5 V dc and +24 V dc for a fully populated board. If only the video and/or auxiliary memory section is being utilized, +24 V dc is not required.

All power to the VIDEO-1 is supplied through terminal block TB1. TB1 is included in the Common Components Kit; refer to the Common Components Assembly paragraph for TB1 installation procedures.

The power and ground wires to the VIDEO-1 must be 16-gage stranded or larger to handle the current required for a fully populated board.

In order to minimize the voltage drop and circuit-induced noise on the power lines, the power and ground wires should be kept as short as possible and should be terminated at the power supply. (That is, run separate +5 V dc, +24 V dc, and ground wires from the power supply to the VIDEO-1 and AIM-65. Do not jumper the power lines from the AIM-65 to the VIDEO-1 or vice versa.)

4.2 AIM-65 INTERCONNECT CABLE

Since the VIDEO-1 uses voltages and signal levels produced by the AIM-65, an interconnect cable must be built before the VIDEO-1 can be assembled.

If the VIDEO-1 is to be installed in the Cedar Rapids AIM User's Group case (now Cedar Valley Computer Association), an interconnect cable approximately 6 in (15 cm) long will be required. For other installations, varying lengths will be required, but in no case should the interconnect cable exceed 3 feet (1 metre) in length.

Standard 26-, 28-, or 30-gage ribbon cable may be used for all signal lines.

4.2.1 Material Required

DESCRIPTION	QUANTITY
Ribbon cable, 44-conductor	6 to 8 inches
Edge connector, 44-pin, 0.156-inch centers	2
Heat-shrink tubing	50 inches

When assembling the interconnect cable, wires will be connected on a one-for-one basis (ie, pin 1 on AIM connector to pin 1 on the VIDEO-1, pin 2 to pin 2, etc).

To assemble the cable and connectors, follow the procedures listed below:

1. Separate and spread the conductors to approximately mate with the solder lugs on the connector.
2. Strip 1/4-in (1 cm) from each conductor of the ribbon cable at both ends, tin the exposed conductor, and slip a 1/2-in (2-cm) piece of heat-shrink tubing over each conductor end, pushing the tubing back to expose the bare wire.
3. Mark one side of one connector "AIM-TOP."
4. Starting with pin 1 of the AIM connector, solder every other conductor of the ribbon cable to the solder lugs on the connector top row.

Note

Do not heat the heat-shrink tubing at this point. When a conductor has been soldered to a lug, wait until the lug is cool before slipping the tubing over. Later trouble-shooting may require the removal of one or more conductors.

5. Mark one side of the other connector "VIDEO-1-TOP."
6. Turn over the AIM connector and ribbon cable so that the side marked "AIM-TOP" is now down.
7. Lay the VIDEO-1 connector so that the side marked "VIDEO-1-TOP" is up. Locate the conductor that is connected to pin 1 on the AIM connector and trace it to the splayed ends. Starting with pin 1, solder every other conductor to the solder lugs in the top row of the VIDEO-1 connector.
8. On the AIM connector, solder the remaining conductors to the bottom row of solder lugs. At this point, examine the AIM connector and ensure that no pins remain unconnected and that no conductors remain unconnected.
9. Turn the cable over and solder the remaining conductors to the bottom row of solder lugs, on the VIDEO-1 connector. Ensure that no pins or conductors remain unconnected.
10. It is recommended that resistance checks be performed between pins on the interconnect cable to ensure that pin 1 is actually connected to pin 1 and so on.
11. After resistance checks are complete, connect the AIM-65 and VIDEO-1 with the interconnect cable and apply +5 V dc, +24 V dc, and ground to the AIM and VIDEO-1. If the AIM does not print "ROCKWELL AIM 65" on power up, check for shorted pins on the

interconnect cable. If the cable checks out OK, do resistance checks between the contacts of the VIDEO-1 J3 connector to ensure that no on-board shorts exist.

12. After verifying the proper operation of the AIM-65 with the blank VIDEO-1 board connected, disconnect the power and interconnect cables from the VIDEO-1 and proceed to the VIDEO-1 assembly section.

4.3 VIDEO-1 ASSEMBLY

The VIDEO-1 has been coated with a solder mask on both sides to minimize the incidence of shorting between circuit runs; however, care must be taken to avoid solder shorts between exposed pads or component leads. Of all the potential problems involved in an assembly of this complexity, solder shorts, unsoldered pins, and cold solder joints are the most difficult to isolate.

When soldering, contact the pad and the lead to be soldered simultaneously. Apply solder to the opposite side of the pad and lead, allowing the solder to fill the hole around the lead. Apply a small amount of additional solder after the space around the lead is filled to produce a solder joint similar in appearance to figure 4-1.

Take care not to move the lead being soldered until the solder has cooled, or a "cold" solder joint (intermittent connection) will result.

Note

Excessive heat can damage the bond between the fiberglass board and the copper pad, resulting in the pad lifting away from the plated-through hole. Do not use larger than a 30-watt soldering iron, and do not expose a pad to heat for longer than 10 seconds while making a solder connection.

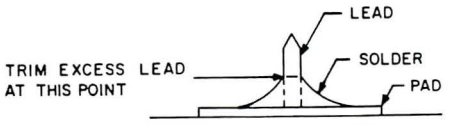


Figure 4-1. Soldering and Lead Trimming.

Axial lead components (components with leads at opposing ends, ie, resistors) should have their leads formed to fit the circuit board holes prior to insertion. Do not bend leads to hold axial components in place; later extraction of a component that has had its leads bent can lift an otherwise good pad.

Note

There are two different types of bypass capacitors (0.1-μF, CPN 913-3279-200) which may have been included in the VIDEO-1 parts kits. Each type must have its leads formed prior to insertion in its mounting holes. Refer to figure 4-2. Type A capacitors must have their leads straightened. Type B capacitors must have a bend made to each lead to reduce the lead spacing.

Cut excess lead lengths just above the solder (see figure 4-1) on all resistors, capacitors, diodes, and transistors. IC socket leads do not require trimming.

Should an assembly error occur which requires a component to be removed, always use a solder sucker to remove excess solder before attempting to remove the component. Failure to do so will cause excessive heat during the removal, which can result in the lifting of a pad and/or associated trace.

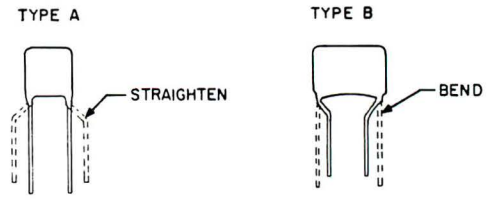


Figure 4-2. Capacitor Lead Forming.

This assembly procedure is broken down into circuit "paragraphs" similar to the parts kits. Refer to the paragraph of the procedure which corresponds to the parts kits you have purchased for specific assembly procedures, starting with the Common Components Assembly paragraph, which follows.

4.3.1 Common Components Assembly

1. Using the Common Components Kit list (see appendix VI), verify that all components have been included in the kit. At this time, also verify the contents of the Socket Kit against the Socket Kit list.
2. Remove from the Common Components Kit the seven stand-offs (CPN 540-9033-003) and seven of the 0.25-inch 4-40 screws (CPN 343-0133-000).
3. Refer to the layout drawings (figures 9-2 through 9-5) to determine on which side of the PCB the components will mount, and insert the screws through the seven mounting holes from the component side and screw them into the seven stand-offs.
4. Set the PCB on your workspace, oriented the same as the layout drawing (standing on the stand-offs).
5. Locate and separate terminal strip TB1 (CPN 367-1599-120) from the Common Components Kit.
6. Refer to the Common Components Layout Drawing and install TB1 by soldering the four contact posts to their respective pads on the back of the VIDEO-1.
7. Locate and separate two 20-pin sockets (CPN 220-0075-080) from the Socket Kit.

Note

Examine one of the sockets and refer to figure 4-3. At one corner of the socket frame, there is a tab which will be used for orienting the integrated circuit (IC) when installing the IC into the socket. The socket should be installed on the PCB so that this tab corresponds to pin 1 as shown on the Components Layout Drawing. Looking at the underside of the socket, you will notice two insulating strips laid over the socket pins. When installing the socket, set the pins into the PCB holes and press firmly to seat the insulating strips against the base of the socket.

After pressing the socket(s) into place on the PCB, lay a sheet of stiff cardboard over the socket(s) (to hold the sockets in place) and invert the board to expose the pins. Solder the opposing corner pins first, and examine the socket to ensure proper seating; then solder the remaining pins.

Note

The printed circuit board must be supported from the rear, when seating components, to avoid undue flexing which can crack circuit traces and cause intermittent operation.

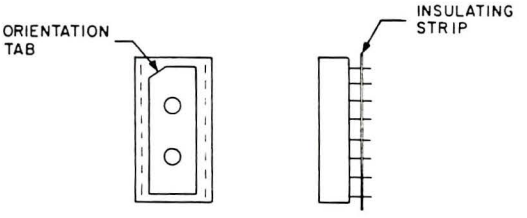


Figure 4-3. Socket Orientation.

8. On the Common Components Layout Drawing, locate integrated circuits U85 and U86. Install the two 20-pin sockets (from step 7) in the holes on the PCB that correspond to U85 and U86 on the layout drawing.
9. Locate and separate two 14-pin sockets (CPN 220-0075-020) from the Socket Kit and install at locations U87 and U98, as shown on the Common Components Layout Drawing.
10. Locate and separate one 16-pin socket (CPN 220-0075-110) from the Socket Kit and install at location U5, as shown on the Common Components Layout Drawing.
11. Locate and separate four 0.1-μF capacitors (CPN 913-3279-200) from the Common Components Kit and install at locations C56, C58, C59, and C60, as shown on the Common Components Layout Drawing.

If only the auxiliary memory portion of the VIDEO-1 is being assembled, proceed to step 16; otherwise, continue with step 12.

12. Remove the 24-pin socket (CPN 220-0075-130) from the Socket Kit and install at location U112.
13. Locate and separate three 16-pin sockets (CPN 220-0075-110) from the Socket Kit and install at locations U7 and U8, as shown on the Common Components Layout Drawing, and at location U118, as shown on the Function Components Layout Drawing.
14. Locate and separate five 14-pin sockets (CPN 220-0075-020) from the Socket Kit and install at locations U9, U10, and U113, as shown on the Common Components Layout Drawing, and locations U119 and U120, as shown on the Function Components Layout Drawing.
15. Locate and separate the remaining six 0.1-μF capacitors (CPN 913-3279-200) from the Common Components Kit and install at locations C57, C61, C62, C63, C64, and C94, as shown on the Common Components Layout Drawing.
16. Plug the interconnect cable onto the AIM-65 at J3, and plug the other end onto the VIDEO-1 J3. Apply power to the AIM and VIDEO-1, and verify the proper operation of the AIM with just the common component sockets installed. If the AIM comes on and resets normally, continue to step 17. If the AIM fails to come up or to run a short program, turn off power, disconnect the VIDEO-1, and check the AIM for proper operation with only the interconnect cable attached. If the AIM operates properly without the VIDEO-1 attached, remove power and check the following on the VIDEO-1:

    a. Examine the circuitry immediately around the components just added for obvious solder bridges. When in doubt, use a solder sucker to remove excess solder.
    b. If no solder bridges were found in the visual inspection, make resistance checks between the address lines on the J3 connector and also between the data and control lines associated with the common decoding circuitry. Check the VIDEO-1 circuits which have low resistance readings. Use a magnifying glass if necessary; some solder shorts are quite small.

17. Prior to inserting an IC into its respective socket, the leads of the IC must be bent to match the row spacing of that socket. When integrated circuits are manufactured, the leads are flared outward for use with autoinsertion equipment. (See figure 4-4A.) This flare must be eliminated in order to insert the IC into a socket (or into the PCB directly) by hand.

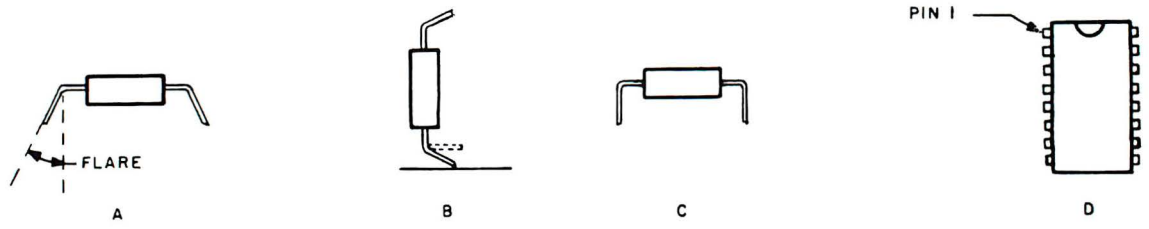


Figure 4-4. Integrated Circuit Preparation.

To correct the IC prior to insertion, grip the IC at each end, lay a row of pins against a firm surface (see figure 4-4B), and press gently, bending all leads until those leads are perpendicular to the IC body. Turn the IC around, and repeat this process with the other row of pins until the IC profile resembles figure 4-4C.

When inserting an IC into its socket, orient the IC so that pin 1 (see figure 4-4D) of the IC corresponds to the orientation tab on the socket, and verify that pin 1 also corresponds to pin 1 as shown on the layout drawing. If an error in socket orientation is found, do not attempt to remove the socket. Instead, place a paint dot on the socket frame next to the true position of pin 1 for future reference. The IC may then be oriented in accordance with the layout drawing.

When installing IC's support the VIDEO-1 from the rear to avoid undue flexing of the circuit board.

18. Remove two 74LS244 IC's (CPN 351-1841-030) from the Common Components Kit and install in the sockets at locations U85 and U86, as shown on the Common Components Layout Drawing.
19. Connect the VIDEO-1 to the AIM-65 via the interconnect cable and apply power. If the AIM operates normally, proceed to step 20. If the AIM fails to operate, turn off AIM power and carefully remove U85 from its socket. Again apply power. If the AIM still does not operate, turn off power, reinsert U85, and remove U86. Apply power. If the AIM powers up normally after the removal of either U85 or U86, the IC removed is suspect. Examine the circuit board immediately around the suspect location for solder shorts and also examine the socket pins for solder shorts or cold solder joints. (Cold solder joints appear dull gray.) If a cold solder joint is located, use a soldering iron to reheat the pad and lead, and, if necessary, apply a small amount of additional solder. If no circuit board faults are located, try another 74LS244 in the suspect location.

20. For the remainder of the Common Components Assembly section, the VIDEO-1 will remain connected to the AIM-65. Always remove power from the system before adding or removing components.

    The U85 and U86 IC's installed in step 18 buffer the address lines servicing the remainder of the decoding circuitry, the EPROM, and the auxiliary memory. Any faults which exist in the address lines to those sections after this point will not cause the AIM to indicate a problem unless a program affecting those areas is initiated.

    Note

    If only the auxiliary memory portion of the VIDEO-1 is being assembled at this time, refer to step 21 and install only U5 and U7. Refer to step 24 and install only U87. Refer to step 25 and install only U98. Proceed from step 25 to the Auxiliary Memory Assembly section.

21. Remove the three 74LS85 IC's (CPN 351-1697-010) from the Common Components Kit and install in the sockets at locations U5, U7, and U8, as shown on the Common Components Layout Drawing.
22. Remove the 74LS30 IC (CPN 351-1523-140) from the Common Components Kit and install in the socket at location U9, as shown on the Common Components Layout Drawing.
23. Remove the 74LS10 IC (CPN 351-1523-230) from the Common Components Kit and install in the socket at location U10, as shown on the Common Components Layout Drawing.
24. Remove the two 74LS00 IC's (CPN 351-1523-110) from the Common Components Kit and install in the sockets at locations U87 and U113, as shown on the Common Components Layout Drawing.
25. Remove two 74LS02 IC's (CPN 351-1523-220) from the Common Components Kit and install in the sockets at location U98, as shown on the Common Components Layout Drawing, and location U120, as shown in the Function Components Layout Drawing.
26. Remove the 74LS138 IC (CPN 351-1526-030) from the Common Components Kit and install at location U118, as shown on the Function Components Layout Drawing.
27. Remove the 74LS32 IC (CPN 351-1523-260) from the Common Components Kit and install in the socket at location U119, as shown on the Function Components Layout Drawing.

The common components installed in steps 18 through 27 above cannot be checked for proper operation without an oscilloscope or without additional components. If an oscilloscope is available, refer to the troubleshooting paragraph, Decoding Circuits, for appropriate waveforms. If no oscilloscope is available, verify that the AIM still powers up normally; then proceed to the next applicable paragraph, Final Assembly.

4.3.2 Video Circuit Assembly

Note

The Common Components Assembly (paragraph 4.3.1) must be completed prior to Video Circuit Assembly.

1. Using the Video Components Kit list (see appendix VI), verify that all required components were included in the kit.

Note

Unless otherwise specified, all component locations in this section are shown on the Video Components Layout Drawing (figure 9-3).

2. Remove three 20-pin sockets (CPN 220-0075-080) from the Socket Kit and install at locations U2, U3, and U4, as shown on the Video Components Layout Drawing.
3. Remove one 16-pin socket (CPN 220-0075-110) from the Socket Kit and install at location U6.
4. Remove the 1000-Ω resistor (CPN 745-0748-000), color-coded brown-black-red, from the Video Components Kit and install at location R1.
5. Remove two 18-pin sockets (CPN 220-0075-090) from the Socket Kit and install at locations U13 and U14.
6. Remove five 0.1-μF capacitors (CPN 913-3279-200), marked "104," from the Video Components Kit and install at locations C9, C15, C16, C17, and C18.
7. Remove one 74LS245 IC (CPN 351-1849-020) from the Video Components Kit and install in the socket at location U2.
8. Remove two 74LS244 IC's (CPN 351-1841-030) from the Video Components Kit and install in the sockets at locations U3 and U4.
9. Remove the 74LS42 IC (CPN 351-1526-050) from the Video Components Kit and install in the socket at location U6.
10. Install two 2114 IC memories (not included) in the sockets at locations U13 and U14.

Note

2114 RAM's are static-sensitive devices. Before handling a 2114 IC, touch a known ground to remove any static buildup from your fingers.

11. Connect the AIM-65 and VIDEO-1, using the interconnect cable, and apply power to the AIM-65 and VIDEO-1.

    Test the circuitry thus far installed by running the memory test listed in appendix VII on memory locations 8000_{16} to 83FF.

    If the memory test is completed successfully, continue to step 12.

    If a fault occurs, the fault indications should be examined to catagorize the type of failure and minimize later troubleshooting. The following categories of faults are not all-inclusive, but they may be used as a guide for general fault isolation.

FAULT INDICATION	PROBABLE FAULT AREA(S)
On power-up, AIM does not respond or will not reset.	• Interconnect wires shorted. • Address lines shorted prior to address buffers. • Data lines shorted prior to data transceiver. • Control lines (02, R/$\overline{W}$) shorted or grounded. • Power lines incorrectly connected (AIM or VIDEO-1).

FAULT INDICATION	PROBABLE FAULT AREA(S)
AIM powers up normally, but VIDEO-1 circuitry does not respond.	• Fault is after the associated address buffers and/or data transceivers, or interconnect has an open circuit. • Power lines incorrectly connected to VIDEO-1.
AIM and VIDEO power up normally, but data is erratic or inconsistent.	• +5 V dc is out of tolerance (4.8 to 5.2 V). • Power lines not terminated at power supply, causing excessive noise on power or ground. • Cold solder joint or unsoldered pin. • Interconnect cable too long.

12. Remove ten 18-pin sockets (CPN 220-0075-090) from the Socket Kit and install at locations U15, U16, U17, U18, U19, U20, U21, U22, U23, and U24.
13. Remove five 0.1-μF capacitors (CPN 913-3279-200) marked "104," from the Video Components Parts Kit and install at locations C10, C11, C12, C13, and C14.
14. Install whatever remaining 2114 IC memories you have alloted to the video area in pairs, running the memory test from appendix VIII before installing the next successive pair.

INSTALL AND	TEST ADDRESSES
U15, U16	8400 - 87FF
U17, U18	8800 - 8BFF
U19, U20	8C00 - 8FFF
U21, U22	9000 - 93FF
U23, U24	9400 - 97FF

Any problems that occur during the installation of the video RAM should be traceable to a given socket, address line, chip select, or data line, depending on the indications provided by the memory test.

15. Remove the 40-pin socket (CPN 220-0075-150) from the Socket Kit and install at location U11.
16. Remove the 0.001-μF capacitor (CPN 913-3281-270), marked "102," from the Video Components Kit. This capacitor (C135) mounts on the rear of the VIDEO-1 in the holes provided between the holes for pins 4 and 11 of U12. Trim the leads of C135 as close to the board surface as possible to avoid interference when the socket for U12 is installed.
17. Remove two 14-pin sockets (CPN 220-0075-020) from the Socket Kit and install at locations U12 and U99.
18. Remove two 20-pin sockets (CPN 220-0075-080) from the Socket Kit and install at locations U1 and U88.
19. Remove the adjustable coil (CPN 242-0447-220) from the Video Components Kit and install at location L1.

Note

If the VIDEO-1 is to be used with composite video output instead of RF, do not install L1.

20. Remove the variable capacitor (CPN 917-1225-000) from the Video Components Kit and install at location C6.
21. Remove the 10,000-Ω potentiometer (CPN 382-0012-290) from the Video Components Kit and install at location R8.
22. Remove the fixed resistors from the Video Components Kit and separate by color coding.
    a. Install the 2,000-Ω resistor (CPN 745-0759-000), color-coded red-black-red, at location R2.
    b. Install the 5600-Ω resistor (CPN 745-0775-000), color-coded green-blue-red, at location R3.
    c. Install the 750-Ω resistor (CPN 745-0744-000), color-coded violet-green-brown, at location R4.
    d. Install the 75-Ω resistor (CPN 745-0708-000), color-coded violet-green-black, at location R5.
    e. Install the two 240-Ω resistors (CPN 745-0726-000), color-coded red-yellow-brown, at locations R6 and R7.
23. Remove the remaining capacitors from the Video Components Kit. These capacitors' locations, unless otherwise specified, are shown on the Video Components Layout Drawing (figure 9-3).
    a. Install the 0.1-μF capacitors (CPN 913-3279-200), marked "104," at locations C1, C3, C4, C19, C20, and C8. (C8 is shown on the Function Components Layout Drawing, figure 9-5.)
    b. Install the 56-pF capacitor (CPN 913-4003-000), marked "560," at location C5.
    c. Install the 0.01-μF capacitor (CPN 913-3281-320), marked "103," at location C7.
    d. Install the 47-pF capacitor (CPN 913-1098-020), marked "470," at location C2.

Note

If the VIDEO-1 is to be used for composite video output instead of RF, do not install C2. In order to produce composite video, C2 must be replaced with a diode. (See figure 4-5.) Coil L1 sets the RF output frequency. The 47-pF capacitor provided in the Video Components Kit provides RF on television channel 4. If channel 4 is being utilized in your viewing area, the aluminum slug in coil L1 may be replaced with a ferrite slug to provide RF output on channel 3.

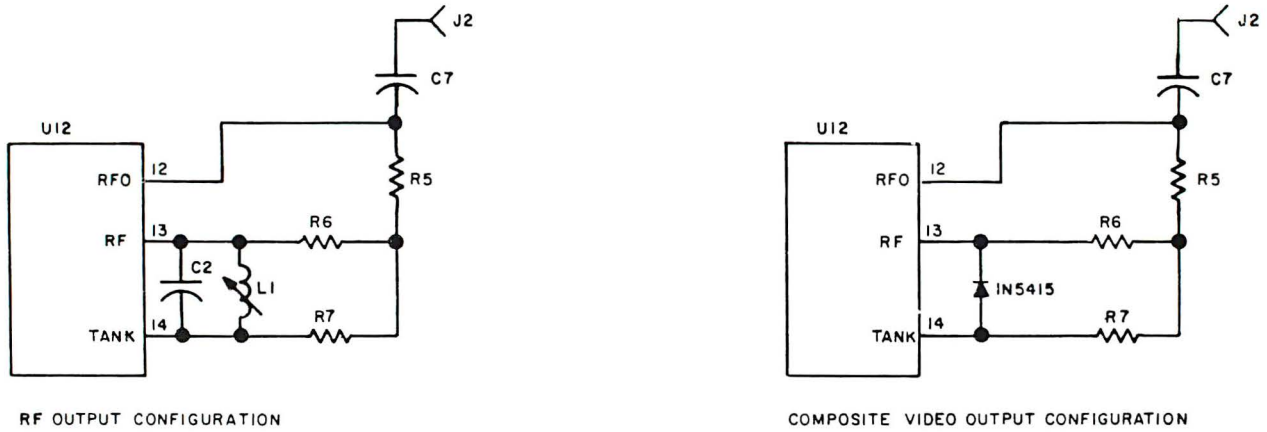


Figure 4-5. Video Output Circuit Differences.

24. If the Function Assembly paragraph was completed prior to the Video Assembly paragraph, proceed to step 26. Remove a 20-pin socket (CPN 220-0075-080) from the Socket Kit and install at location U117, as shown on the Function Components Layout Drawing.
25. Remove the 74LS245 IC (CPN 351-1849-020) from the Video Components Kit and install at location U117.
26. Crystal Y1 is not provided with the VIDEO-1 and must be procured locally. Y1 is a standard 3.579545-MHz color-burst crystal available at television repair shops or electronics retailers.

    Preform the leads or Y1 by gripping each lead with needle-nose pliers next to the crystal case and then bending the leads 90 degrees. Install Y1 as shown on the Video Components Layout Drawing (figure 9-1).
27. Remove the mounting bracket (CPN 763-7388-004), two 0.25 4-40 screws (CPN 343-0133-000) and two 4-40 nuts (CPN 313-0132-000) from the Video Components Kit, and install the bracket at the board edge between J1 and J3, using the screws and nuts.

Note

If the VIDEO-1 is to be installed in the shallow base of the case provided by Rockwell, do not install the mounting bracket. Instead, mount the RCA phono jack directly onto the rear of the case.

28. Remove the RCA phono jack (no CPN) from the Video Components Kit and install on the mounting bracket, using the ground lug and nut provided.
29. Procure a 2-inch length of subminiature coaxial cable (not provided) and strip approximately 1/2 inch of insulation from the shield at one end. Carefully separate the braided shielding and strip 1/4 inch of the insulation from the center conductor. Twist the shielding to form a stranded wire for later connection to the ground lug on J2.

    At the other end of the coaxial cable, strip 1/4 inch of insulation and shield from the center conductor. Strip 1/8 inch of insulation from center conductor, and tin the exposed end.

    Slip a 1/2-inch piece of heat-shrink tubing over the tinned end of the coaxial cable (to ensure that the ends of the stripped-off shield cannot contact other components), and shrink.
30. Insert the tinned center conductor into the plated-through hole next to C7 (between the pads used for R4 and R5 leads), and solder in place.
31. Solder the other end of the coaxial cable to the center lug on J2. The shield should be soldered to the grounding lug of J2.
32. Remove the MC6847 IC (CPN 128-0076-001) from the Video Components Kit and install at location U11, as shown on the Video Components Layout Drawing. (Do this carefully, as the leads can be bent during insertion if they are not all aligned with the socket holes.)
33. Remove the MC1372 IC (CPN 128-0076-002) from the Video Components Kit and install at location U12, as shown on the Video Components Layout Drawing.
34. Remove the 74LS00 IC (CPN 351-1523-110) from the Video Components Kit and install at location U99, as shown on the Video Components Layout Drawing.
35. Remove the 74LS374 IC (CPN 351-1821-030) from the Video Components Kit and install at location U1, as shown on the Function Components Layout Drawing.
36. Remove the 74LS244 IC (CPN 351-1841-030) from the Video Components Kit and install at U88, as shown on the Function Components Layout Drawing.

This completes the Video Assembly.

4.3.3 Video Alignment

1. Connect the AIM-65 to the VIDEO-1 with the interconnect cable.
2. For RF operation with a standard black and white or color television:

   a. Connect a 75-Ω coaxial cable from VIDEO-1 connector J2 to either a video game box (game input) or to a 75- to 300-Ω antenna terminator (75-Ω input).
   b. Connect the 300-Ω output of the game box or antenna terminator to the VHF input terminals of a standard television.
3. For video operation with a video monitor or modified television, connect a 75-Ω coaxial cable from VIDEO-1 connector J2 to the video input connector of the video monitor or the IF input of a modified television.

Note

L1 and C2 must be replaced with a diode for video output from J2.

4. Apply +5 V dc to the AIM-65 and VIDEO-1 (+24 V dc is not required for video operation.)
5. Press "M," type "9FFF," press "RETURN," "1," and type "00." This places the VIDEO-1 in the alphanumerics mode. This location is a latch and cannot be read. The AIM-65 will therefore respond, "MEMORY FAIL."
6. If the television is equipped with automatic fine tuning, disable the AFC. Set the television for channel 4.
7. Set the duty cycle adjust (R8) on the VIDEO-1 to midpoint. (R8 is a 15-turn potentiometer.)
8. Using a nonmetallic tuning tool, adjust L1 until a rectangular field of random letters, numbers, and symbols appears on the television screen.
   a. Coil L1 has an aluminum tuning slug. The further the slug is inserted into the coil, the less inductance is realized; therefore, the frequency increases.
   b. If the rectangular field is not attainable by adjusting L1, adjust the manual fine tuning of the television through its range on channels 3, 4, and 5, looking for the transmitted signal.
   c. If still no field is seen, adjust C6 90 degrees (either clockwise or counterclockwise) and again adjust L1 and search channels 3, 4, and 5 until the field is located.
9. Once the field is located, adjust L1 to center the signal in channel 4.
10. Enter and run the following BASIC program:

```
10 FOR X = 0 TO 512
20 POKE (32768 + X), INT (X/2)
30 NEXT
```

    This program will fill the screen with pairs of letters, numbers, and symbols, both normal and inverted.
11. Examine the characters on the screen. If any character is out of proportion or blurred, adjust R8 to correct.
12. If the VIDEO-1 is being used with a color television, capacitor C6 is used to adjust the tint.
13. To test the mode latches, enter and run the following BASIC program:

```
100 FOR Y = 0 TO 255
110 POKE 40959, Y
120 FOR Z = 0 TO 200
130 NEXT Z
140 NEXT Y
```

    This program will step through the various modes of the VIDEO-1.

4.3.4 Auxiliary Memory Assembly

Note

The Common Components Assembly must be performed prior to the Auxiliary Memory Assembly.

1. Verify the contents of the Auxiliary Memory Components Kit using the Auxiliary Memory Components Kit list in appendix VI.
2. Unless otherwise stated, refer to the Auxiliary Memory Components Layout Drawing (figure 9-4) for the location of the components listed in this assembly paragraph.
3. Remove two 20-pin sockets (CPN 220-0075-080) from the Socket Kit and install at locations U103 and U116.
4. Remove one 16-pin socket (CPN 220-0075-110) from the Socket Kit and install at location U25.
5. Remove two 18-pin sockets (CPN 220-0075-090) from the Socket Kit and install at locations U27 and U28.
6. Remove three 0.1-μF capacitors (CPN 913-3279-200) from the Auxiliary Memory Components Kit and install at locations C22, C50, and C51.
7. Remove the 74LS244 IC (CPN 351-1841-030) from the Auxiliary Memory Components Kit and install in the socket at location U103.
8. Remove the 74LS245 IC (CPN 351-1849-020) from the Auxiliary Memory Components Kit and install in the socket at location U116.
9. Remove one 74LS138 IC (CPN 351-1526-030) from the Auxiliary Memory Components Kit and install in the socket at location U25.
10. Install two 2114 RAM IC's (not included) in the sockets at locations U27 and U28.
11. Connect the VIDEO-1 to the AIM-65 with the interconnect cable and apply +5 V dc. (+24 V dc is not required for auxiliary memory operation.)
12. Enter and run the memory test program listed in appendix VII on addresses 1000 to 13FF. If the memory test is completed successfully, continue with step 13. If a fault occurs, do not install further sockets or IC's; refer to the troubleshooting paragraph for the appropriate procedures.
13. Remove the remaining 0.1-μF capacitors from the Auxiliary Memory Components Kit and install at locations C23-C49 and C52-C55.
14. Remove the remaining three 16-pin sockets (CPN 220-0075-110) from the Socket Kit and install at locations U26, U83, and U84.
15. Remove the remaining fifty-four 18-pin sockets (CPN 220-0075-090) from the Socket Kit and install at locations U29-U82.
16. Remove the three 74LS138 IC's (CPN 351-1526-030) from the Auxiliary Memory Components Kit and install in the sockets at locations U26, U83, and U84.
17. Install the remaining 2114 RAM IC's in pairs, starting with locations U29 and U30. Run the memory test listed in appendix VIII on each pair of 2114 IC's before installing the next pair. Refer to table 2-2 for a listing of RAM locations and corresponding addresses.

4.3.5 Digital-to-Analog, Analog-to-Digital, and Light Pen Assembly

Note

The Common Components Assembly paragraph must be performed prior to the D/A, A/D, and Light Pen Assembly paragraph.

1. Verify the contents of the D/A, A/D, Light Pen Components Kit, using the D/A, A/D, Light Pen Components Kit list in appendix VI.
2. This section will assemble the analog portion of the VIDEO-1 in the following sequence:

   a. Power Supply.
   b. Digital-to-Analog Converter No. 1.
   c. Digital-to-Analog Converter No. 2.
   d. Analog-to-Digital Converter.
   e. Light Pen Ciircuitry and Light Pen.

   The alignment of the analog circuitry is based on the above sequence. For the locations of the components in this section, refer to the Function Components Layout Drawing (figure 9-5).

4.3.5.1 Power Supply Assembly

1. Remove the LM340T-15 3-leg regulator (CPN 351-1120-050) from the Function Components Kit. Carefully bend the leads 90 degrees from the body and mount flat at location U114. Make sure that the hole in the heat-sink tab of U114 mates with the hole in the printed circuit board before soldering the leads.
2. Remove the 0.25-inch 4-40 screw (CPN 343-0133-000) and nut (CPN 313-0132-000) from the Function Components Kit. Insert the screw through the hole in the heat-sink tab and PCB, and secure it with the nut.

Note

For improved heat-sinking of U114, apply a small amount of heat-sink compound to the underside of the heat-sink tab before installing the mounting screw and nut.

3. Remove one 8-pin socket (CPN 220-0075-010) from the Function Components Kit and install at location U115.
4. Remove the three 1N5415 diodes (CPN 353-6558-010) from the Function Components Kit and install at locations CR1, CR2, and CR3. The cathode end of each diode has a painted stripe which must correspond to the banded end shown on the Function Components Layout Drawing.
5. Remove the 2N2222A transistor (CPN 352-0661-020) from the Function Components Kit and install at location Q1.
6. Remove the 2N2907A transistor (CPN 352-0551-010) from the Function Components Kit and install at location Q2.
7. Remove the 0.1-μH coil (CPN 240-2715-010) from the Function Components Kit and install at location L2. (L2 is a fixed coil and looks like a 1/2-watt resistor with a green body.)

8. The following fixed resistors are in the Function Components Kit:

   a. Install two 2,000-Ω, 1/8-watt resistors (CPN 745-1863-560), color-coded red-black-red, at locations R15 and R17.
   b. Install a 120-Ω, 1/8-W resistor (CPN 745-1863-270), color-coded brown-red-brown, at location R19.
   c. Install a 240-Ω, 1/8-W resistor (CPN 745-1863-340), color-coded red-yellow-brown, at location R13.
   d. Install the 1-W, 45.3-Ω resistor (CPN 747-2178-970) at location R16. R16 is the largest resistor in the kit and has no color coding. (The number 453 will be stamped on the body of R16.)

9. The following trimmer potentiometers are in the Function Components Kit:

   a. Install a 2,000-Ω trimmer (CPN 382-0012-270) at location R20.
   b. Install a 5,000-Ω trimmer (CPN 382-0012-280) at location R14.

10. The following capacitors are in the Function Components Kit:

   a. Install two 0.01-μF capacitors (CPN 913-3279-110), marked "103," at locations C70 and C71.
   b. Install four 0.1-μF capacitors (CPN 913-3279-200), marked "104," at locations C69, C130, C131, and C132.
   c. Install the 15-μF capacitor (CPN 184-9086-490) at location C72. (C72 is a silver tubular electrolytic capacitor.) Be sure to orient the plus end of C72 as shown on the Function Components Layout Drawing.
   d. The remaining capacitors in the power supply, tantalum and polarity, must be observed in their installation. Tantalum capacitors, if installed backwards, can be damaged when power is initially applied. The positive lead of each capacitor will be marked with either a plus (+) or a red dot. Orient the positive lead of the capacitor as shown by the plus on the Function Components Layout Drawing.
   e. Install the 35-V, 47-μF capacitor (CPN 184-9102-890) at location C66.
   f. Install the 20-V, 47-μF capacitor (CPN 184-9102-190) at location C67.
   g. Install the three 20-V, 10-μF capacitors (CPN 184-9102-170) at locations C68, C73, and C74.

11. Remove the LM317MP (CPN 128-0076-005) and LM337MP (CPN 128-0076-007) 3-leg regulators from the Function Components Kit. Refer to figure 4-6, and bend the heat-sink tab 90 degrees from the body of each, away from the chamfered corners.
12. Install the LM317MP at location U125. The banded side of U125 on the Function Components Layout Drawing corresponds to the flat (nonchamfered) side of the LM317MP.
13. Install the LM337MP at location U126. The banded side of U126 on the Function Components Layout Drawing corresponds to the flat side of the LM337MP.
14. Remove the two LM340LAZ-5 3-leg regulators (CPN 128-0076-006) from the Function Components Kit and install at locations U127 and U128. (The LM340LAZ-5 and LM320LZ-5 look like plastic case transistors.)
15. Remove the LM320LZ-5 3-leg regulator (CPN 128-0076-008) from the Function Components Kit and install at location U129.

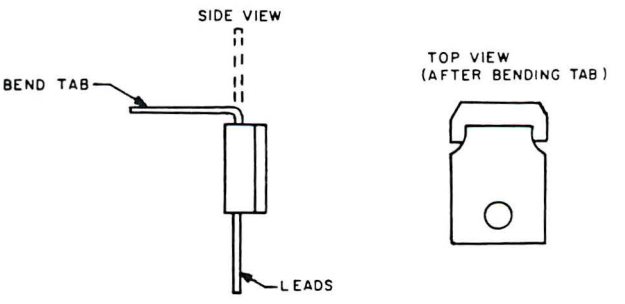


Figure 4-6. Heat-Sink Tab-Bending Information.

16. Apply +24 V dc to VIDEO-1 terminal strip TB1. (The AIM-65 need not be connected for the following tests.) With a voltohmmeter, check the voltage at the plus (+) side of C67. If the voltage present at C67 is 15 V dc ±1 V, proceed to step 17. If the voltage at C67 is wrong or absent, verify that C66 and C67 are properly oriented. If C66 and C67 are correctly installed, U114 is suspect. Before replacing U114, however, check the circuitry around TB1, U114, and U115 for solder shorts or cold solder joints. Also check to ensure that the connections at TB1 are correct.
17. With +24 V dc still applied, check the voltage at the plus (+) side of C68. The voltage at C68 should be between 0 and +15 V dc. Adjust trimmer potentiometer R14 to set the voltage at C68 to +8 V dc ±0.1 V. If no voltage is present at C68 or adjustment of R14 does not vary the voltage at C68, check the polarity of C68. Also check U125 to ensure that it is an LM317MP. (It is possible to confuse U125 and U126.)
18. Check the voltage at J1, pin K. This voltage should be +5 V dc ±0.1 V. If it is not, check U128 to ensure that it is an LM340LAZ-5. Also check the circuitry around U128.
19. Check the voltage at R12. R12 should have +5 V dc ±0.1 V on either end. If not, check U127 to ensure that it is an LM340LAZ-5. Also check the circuitry immediately around U127 for solder shorts or cold solder joints.
20. Remove power from the VIDEO-1. Remove the 555 IC's (CPN 351-1137-020) from the Function Components Kit and install in the socket at location U115.
21. Apply +24 V dc to the VIDEO-1. Using a VOM, verify the presence of +15 V dc on pin 8 of U115.
22. Check the voltage at the minus (-) side of C74. The voltage at C74 should be between 0 and -10 V dc. Adjust trimmer potentiometer R20 to set the voltage at C74 to -8 V dc ±0.1 V.
23. Verify the presence of -5 V dc at pin 2 of regulator U129.
24. Remove power from the VIDEO-1, and proceed to Digital-to-Analog Converter No. 1 assembly.

4.3.5.2 Digital-to-Analog Converter No. 1 Assembly

1. If the Video Assembly paragraph was completed prior to this point, proceed to step 5.
2. Remove one 20-pin socket (CPN 220-0075-080) from the Socket Kit and install at location U117.
3. Remove the 74LS245 IC (CPN 351-1849-020) from the Function Components Kit and install in the socket at location U117.
4. Connect the AIM-65 and VIDEO-1 with the interconnect cable and apply +5 V dc to the system. Verify proper AIM-65 operation with U117 installed.
5. Remove two 20-pin sockets (CPN 220-0075-080) from the Socket Kit and install at locations U104 and U105.
6. Remove two 16-pin sockets (CPN 220-0075-110) from the Socket Kit and install at locations U107 and U110.
7. Remove one 8-pin socket (CPN 220-0075-010) from the Socket Kit and install at location U109.
8. Remove nine 0.1-μF capacitors (CPN 913-3279-200), marked "104," from the Function Components Kit and install at locations C75, C80, C81, C90, C99, C107, C108, C113, and C116.
9. Remove one 15-pF capacitor (CPN 912-4141-130), marked "15" or "150," from the Function Components Kit and install at location C76.
10. Remove one 68-pF capacitor (CPN 912-4141-330), marked "68" or "680," from the Function Components Kit and install at location C79.
11. Remove two 47-Ω, 1/8-W resistors (CPN 745-1863-170), color-coded yellow-violet-black, from the Function Components Kit and install at locations R58 and R59.
12. Remove three 3,000-Ω, 1/8-W resistors (CPN 745-1863-600), color-coded orange-black-red, from the Function Components Kit and install at locations R22, R23, and R24.

13. Remove one 1,500-Ω, 1/8-W resistor (CPN 745-1863-530), color-coded brown-green-red, and install at location R45.
14. Remove one 5,000-Ω trimmer potentiometer (CPN 382-0012-280) from the Function Components Kit and install at location R21.
15. Remove one 1-MΩ resistor network (CPN 350-4030-150) from the Function Components Kit. (The resistor networks are 16-pin dual-in-line packs similar to IC's.) Install the resistor network at location R42, ensuring that the pin marked "1" corresponds to pin 1 on the Function Components Layout Drawing.
16. Remove two 74LS374 IC's (CPN 351-1821-030) from the Function Components Kit and install in the sockets at locations U104 and U105.
17. Remove one 1408 IC (CPN 351-1152-010) from the Function Components Kit and install in the socket at location U107.
18. Remove one LM356N IC (CPN 351-1287-040) from the Function Components Kit and install in the socket at location U109.
19. Remove one 4051 IC (CPN 351-8236-010) from the Function Components Kit.

CAUTION

THE 4051 IS A CMOS DEVICE, SENSITIVE TO STATIC DISCHARGE. CONTACT A LOCAL GROUND BEFORE HANDLING ANY CMOS DEVICE.

Install the IC in the socket at location U110.

20. Connect the AIM-65 and VIDEO-1 with the interconnect cable, and apply both +5 V dc and +24 V dc to the system.
21. On the AIM-65 keyboard, press "M," type "9FF9," press "RETURN," "1," and type "00." This step initializes D/A No. 1 output multiplexer to enable output 0 at connector J1-F.
22. Press "M," type "9FFA," press "RETURN," "1," and type "FF." This step provides the maximum dc output from D/A No. 1.

Note

In both step 21 and 22, above, the AIM-65 will respond "MEMORY FAIL" after data is entered. Addresses 9FF9, 9FFA, 9FFB, and 9FFF are write-only latches. The AIM Monitor reads any address changed immediately after writing to it. The write-only latches present a high impedance to the data lines, and the AIM-65 interprets this high impedance as "FF."

23. Using a DVM or VOM, check the voltage at connector J1, pin F. Adjust potentiometer R20 for +2.56 V dc at J1-F. This adjustment sets the step voltage from D/A No. 1 to 10 mV. Potentiometer R20 may be used to specify the D/A No. 1 output to other levels to satisfy user requirements.

If an oscilloscope is available, the following programs may be used to generate an observable ramp from D/A No. 1:

a.
```
0000   INY
       STY   9FFA
       JMP   0000
```

b.
```
10    FOR X = 0 TO 255
20    POKE 40953, X
30    NEXT
40    GOTO 10
```

24. If any problems occurred in the performance of steps 21 through 23, above, refer to the troubleshooting paragraph.

4.3.5.3 Digital-to-Analog Converter No. 2 Assembly

1. Remove two 20-pin sockets (CPN 220-0075-080) from the Socket Kit and install at locations U96 and U106.
2. Remove three 16-pin sockets (CPN 220-0075-110) from the Socket Kit and install at locations U108, U111, and U122.
3. Remove one 8-pin socket (CPN 220-0075-010) from the Socket Kit and install at location U130.
4. Remove eleven 0.1-μF capacitors (CPN 913-3279-200), marked "104," from the Function Components Kit and install at locations C82, C84, C100, C101, C105, C106, C117, C118, C121, C122, and C134.
5. Remove one 15-pF capacitor (CPN 912-4141-130) from the Function Components Kit and install at location C83.
6. Remove one 68-pF capacitor (CPN 912-4141-330) from the Function Components Kit and install at location C86.
7. Remove three 3,000-Ω, 1/8-W resistors (CPN 745-1863-600) from the Function Components Kit and install at locations R28, R29, and R30.
8. Remove two 47-Ω, 1/8-W resistors (CPN 745-1863-170) from the Function Components Kit and install at locations R60 and R61.
9. Remove one 1,500-Ω, 1/8-W resistor (CPN 745-1863-530) from the Function Components Kit and install at location R54.
10. Remove one 5,000-Ω trimmer potentiometer (CPN 382-0012-280) from the Function Components Kit and install at location R25.
11. Remove one 10,000-Ω trimmer potentiometer (CPN 382-0012-290) from the Function Components Kit and install at location R26.
12. Remove one 1-MΩ resistor network (CPN 350-4030-150) and install at location R43.
13. Remove two 74LS374 IC's (CPN 351-1821-030) from the Function Components Kit and install in the sockets at locations U96 and U106. (U96, while not required for D/A operation, must be installed at this stage to provide the proper input loading for U122.)
14. Remove one 1408 IC (CPN 351-1152-010) from the Function Components Kit and install in the socket at location U108.
15. Remove one LM356N (CPN 351-1287-040) from the Function Components Kit and install in the socket at location U130.
16. Remove one 4051 CMOS IC (CPN 351-8236-010) from the Function Components Kit and install in the socket at location U111.
17. Remove one 4053 CMOS IC (CPN 351-8236-020) from the Function Components Kit and install in the socket at location U122.
18. Connect the AIM-65 and VIDEO-1 with the interconnect cable and apply both +5 V dc and +24 V dc to the system.
19. Press the "M" key, type "9FF9," and press "RETURN."
20. Press the "/" key and type "80." The AIM will store 80_{16} at address $9FF9_{16}$ and respond "MEMORY FAIL." Storing 80_{16} at $9FF9_{16}$ will enable D/A No. 2 output to connector J1, pin N, and provide the V_{REF} to U108 via potentiometer R25.
21. Press the "M" key again, type "9FFB," and press "RETURN."
22. Press the "/" key and type "80." The AIM will store 80_{16} in D/A No. 2, latch U106, and respond "MEMORY FAIL."

23. Using a VOM, measure the voltage at J1, pin N.
24. Adjust potentiometer R26 for 0 V at J1-N.
25. Press "/" and type "FF." The AIM will respond "MEMORY FAIL."
26. Measure the voltage at J1-N, and adjust R25 to set that voltage at +2.5 V dc, ±0.1 V.
27. Press the "/" key and type "00." The AIM will respond "MEMORY FAIL."
28. Verify the presence of -2.5 V dc at J1-N.
29. If any problems occur while performing steps 19 through 28, above, refer to the trouble-shooting paragraph.

4.3.5.4 Analog-to-Digital Converter Assembly

1. Remove one 20-pin socket (CPN 220-0075-080) from the Socket Kit and install at location U102.
2. Remove five 16-pin sockets (CPN 220-0075-110) from the Socket Kit and install at locations U93, U95, U100, U101, and U123.
3. Remove two 14-pin sockets (CPN 220-0075-020) from the Socket Kit and install at locations U89 and U121.
4. Remove four 8-pin sockets (CPN 220-0075-010) from the Socket Kit and install at locations U94, U97, U124, and U131.
5. Remove twenty-six 0.1-μF capacitors (CPN 913-3279-200), marked "104," from the Function Components Kit and install at locations C55, C77, C78, C87, C88, C89, C91, C93, C96, C97, C102, C103, C109, C110, C111, C112, C114, C115, C119, C120, C123, C124, C126, C127, C128, and C129.
6. Remove one 15-pF capacitor (CPN 912-4141-130), marked "15" or "150," from the Function Components Kit and install at location C92.
7. Remove one 68-pF capacitor (CPN 912-4141-330), marked "68" or "680," from the Function Components Kit and install at location C95.
8. Remove one 82-pF capacitor (CPN 912-4141-350), marked "82" or "820," from the Function Components Kit and install at location C98.
9. Remove six 47-Ω, 1/8-W resistors (CPN 745-1863-170), color-coded yellow-violet-black, from the Function Components Kit and install at locations R27, R62, R63, R64, R65, and R66.
10. Remove three 4,700-Ω, 1/8-W resistors (CPN 745-1863-650), color-coded yellow-violet-red, from the Function Components Kit and install at locations R38, R47, and R55.
11. Remove three 3,000-Ω, 1/8-W resistors (CPN 745-1863-600), color-coded orange-black-red, from the Function Components Kit and install at locations R33, R34, and R35.
12. Remove three 10,000-Ω, 1/8-W resistors (CPN 745-1863-730), color-coded brown-black-orange, from the Function Components Kit and install at locations R39, R40, and R48.
13. Remove two 20-Ω, 1/8-W resistors (CPN 745-1863-080), color-coded red-black-black, from the Function Components Kit and install at locations R56 and R57.
14. Remove one 1,000-Ω, 1/8-W resistor (CPN 745-1863-490), color-coded brown-black-red, from the Function Components Kit and install at location R41.
15. Remove one 1,500-Ω, 1/8-W resistor (CPN 745-1863-530), color-coded brown-green-red, from the Function Components Kit and install at location R67.
16. Remove one 27,000-Ω, 1/8-W resistor (CPN 745-1863-830), color-coded red-violet-orange, from the Function Components Kit and install at location R36.
17. Remove one 2,400-Ω, 1/8-W resistor (CPN 745-1863-580), color-coded red-yellow-red, from the Function Components Kit and install at location R46.
18. Remove one 36,000-Ω, 1/8-W resistor (CPN 745-1863-860), color-coded orange-blue-orange, from the Function Components Kit and install at location R49.
19. Remove one 150,000-Ω, 1/8-W resistor (CPN 745-1864-050), color-coded brown-green-yellow, from the Function Components Kit and install at location R50.

20. Remove one 300,000-Ω, 1/8-W resistor (CPN 745-1864-120), color-coded orange-black-yellow, from the Function Components Kit and install at location R51.
21. Remove one 100,000-Ω trimmer potentiometer (CPN 382-0012-330) from the Function Components Kit and install at location R37.
22. Remove one 1-MΩ trimmer potentiometer (CPN 382-0012-370) from the Function Components Kit and install at location R52.
23. Remove one 20,000-Ω trimmer potentiometer (CPN 382-0012-300) from the Function Components Kit and install at location R53.
24. Remove one 10,000-Ω trimmer potentiometer (CPN 382-0012-290) from the Function Components Kit and install at location R32.
25. Remove one 5,000-Ω trimmer potentiometer (CPN 382-0012-280) from the Function Components Kit and install at location R31.

Note

Before applying power to the VIDEO-1, adjust potentiometers R31, R32, R37, R52, and R53 to midpoint. (These potentiometers are 15-turn with click end-stops; turn each potentiometer until a faint click is heard, and turn back seven turns.)

26. Remove one 1-MΩ resistor network (CPN 350-4030-150) from the Function Components Kit and install at location R44.
27. Remove two 4051 CMOS IC's (CPN 351-8236-010) from the Function Components Kit and install in the socket at locations U93 and U95.
28. Remove three LM356N IC's (CPN 351-1287-040) from the Function Components Kit and install in the sockets at locations U94, U131, and U97.
29. Remove the LM318 IC (CPN 351-1153-040) from the Function Components Kit and install in the socket at location U124.
30. Remove the LM319 IC (CPN 351-1166-010) from the Function Components Kit and install in the socket at location U89.
31. Remove the 74LS123 IC (CPN 351-1699-020) from the Function Components Kit and install in the socket at location U123.
32. Remove the 2502 IC (CPN 128-0076-003) from the Function Components Kit and install in the socket at location U100.
33. Remove the 74LS00 IC (CPN 351-1523-110) from the Function Components Kit and install in the socket at location U121.
34. Remove the 1408 IC (CPN 351-1152-010) from the Function Components Kit and install in the socket at location U101.
35. Remove one 74LS374 IC (CPN 351-1821-030) from the Function Components Kit and install in the socket at location U102.

This completes the Analog-to-Digital Converter Assembly.

4.3.5.5 Analog-to-Digital Converter Alignment

1. On the J1 connector, temporarily connect pin F to pin 17 (D/A No. 1 output 0 to A/D input 0), and connect pin T to pin 21 (A/D input 1 to analog ground). Push connector J1 onto edge connector J1.
2. Connect the AIM-65 and VIDEO-1 with the interconnect cable.

3. Apply +5 V dc and +24 V dc to the AIM-65 and VIDEO-1, and initialize the D/A and A/D sections in the following sequence:

   a. Press "M," type "9FF9," and press "RETURN." Press "/" and type "00."
   b. Press "M," type "9FFA," and press "RETURN." Press "/" and type "80."
   c. Press "M," type "9FFC," and press "RETURN." Press "/" and type "0F."

   The above sequence enables D/A No. 1 output 0 (step a), provides a +2.5-V dc output from D/A No. 1 (step b), enables A/D input 0, sets a fixed offset for the A/D, and establishes the gain of the A/D preamplifier (step c).

4. Measure and note the voltage present at U93, pin 13, and at U97, pin 6.
5. Press "/" and type "1F." This changes the A/D input to channel 1, which has been grounded on connector J1.
6. Measure and note the voltage present at U93, pin 3, and at U97, pin 6.
7. The voltage difference between the measurements taken at U93, pin 3, in steps 4 and 6 should equal the difference between the measurements taken at U97, pin 6, in steps 4 and 6. If the Δ voltage is not the same, adjust R53 and measure by pressing "/" and typing either "0F" (to enable input 0) or "1F" (to enable input 1). Repeat and adjust R53 until the Δ voltage at U93, pin 3, and U97, pin 6, are equal.

   The above procedure establishes a precision unity gain preamplifier for the A/D converter.
8. Press "/" and type "1F" to enable input 1. Adjust R37 until the output of U97 (pin 6) is 0 V ±0.01 V dc. This step sets the fixed offset of U131.
9. Turn off the power to the system, and remove the jumper on the connector from J1, pin F, to J1, pin 17. Add a jumper from J1, pin N, to J1, pin 17. (This connects D/A No. 2 output 0 to input 0 of the A/D.)
10. Again apply both +5 V dc and +24 V dc to the system, and initialize the D/A and A/D sections in the following sequence:

    a. Press "M," type "9FF9," and press "RETURN." Press "/" and type "80."
    b. Press "M," type "9FFB," and press "RETURN." Press "/" and type "00."
    c. Press "M," type "9FFC," and press "RETURN." Press "/" and type "0F."

    The above sequence enables D/A No. 2 output 0 and provides a fixed offset to D/A No. 2 (step a); provides a -2.5-V dc output from D/A No. 2 (step b); and enables A/D input 0, sets a fixed offset for the A/D, and selects the precision unity gain setting for the A/D preamplifier (step c).

11. Enter the following program into the AIM-65:

```
0000    LDA    9FFC
0003    NOP
0004    NOP
0005    NOP
0006    LDA    9FFC
0009    JSR    EA46
000C    JSR    EA13
000F    JMP    0200
```

12. Turn off the AIM-65 printer, and run the program entered in step 11. This program displays the hexadecimal value of the A/D output on the AIM-65 display.

    Adjust potentiometer R32 while watching the AIM display until the displayed number transitions from 01 to 00. Adjust R32 back and forth until the display just transitions to 00.
13. Reset the AIM-65, press "M," type "9FFB," and press "RETURN." Press "/" and type "80."
14. Run the program entered in step 11. Adjust R31 until the AIM displays "80."
15. Reset the AIM-65, press "M," type "9FFB," and press "RETURN." Press "/" and type "FF."
16. Run the program entered in step 11. Verify that the display shows "FF."
17. Repeat steps 11 through 16 until the display consistently displays "00," "80," and "FF" at the appropriate steps.
18. If problems are encountered in the performance of steps 3 to 17 (above), refer to the troubleshooting paragraph.

4.3.5.6 Light Pen Assembly

1. Remove one 16-pin socket (CPN 220-0075-110) from the Socket Kit and install at location U90.
2. Remove two 20-pin sockets (CPN 220-0075-080) from the Socket Kit and install at locations U91 and U92.
3. Remove two 0.1-μF capacitors (CPN 913-3279-200), marked "104," from the Function Components Kit and install at locations C85 and C133.
4. Remove two 100-Ω, 1/8-W resistors (CPN 745-1863-250), color-coded brown-black-brown, from the Function Components Kit and install at locations R11 and R12.
5. Remove one 1,000-Ω resistor (CPN 745-1863-490), color-coded brown-black-red, from the Function Components Kit and install at location R9.
6. Remove one 10,000-Ω trimmer potentiometer (CPN 382-0012-290) from the Function Components Kit and install at location R10.
7. Remove the two remaining 74LS374 IC's (CPN 351-1821-030) from the Function Components Kit and install at locations U91 and U92.
8. Remove one 74LS112 IC (CPN 351-1525-030) from the Function Components Kit and install at location U90.
9. Remove the MRD 370 photo Darlington transistor (CPN 128-0076-004), the length of shielded, twisted pair wire (CPN 439-0650-000), and the aluminum tube (CPN 804-3084-022) from the Function Components Kit.
10. Strip 1-1/2 in (6 cm) of insulation from one end of the twisted, shielded pair to expose the shield. Carefully fold the shielding back over the insulation to expose the twisted pair as shown in figure 4-7. Tape the splayed ends of the shield to the insulation. Strip 1/4 in (1 cm) of insulation from each of the exposed wires, and tin the leads.

    The folded-back shield is intended to contact the inside of the aluminum light pen tube to ground the tube itself. The tube must be grounded to shield the light pen photocell from the field produced by the flyback transformer inside the television. Failure to properly ground the light pen tube will result in the light pen attempting to latch on nonexistent data during horizontal retrace.
11. Referring to figure 4-8, cut the base lead of the MRD 370 (Q3) 1/2 in (2 cm) from the case, and cover with heat-shrink tubing. Cut the collector and emitter leads 1 in (4 cm) from the case.

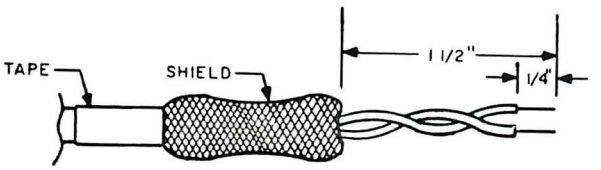


Figure 4-7. Shielded, Twisted Pair Preparation.

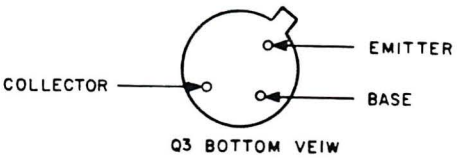


Figure 4-8. Q3, Bottom View.

12. Heat sink the collector lead of Q3 next to the case with an alligator clip or needlenose pliers. Slip a 1-1/4-in (5-cm) piece of heat-shrink tubing over the red lead of the twisted pair, and solder the red lead to the collector lead of Q3.
13. Heat sink the emitter lead of Q3 next to the case. Slip a 1-1/4-in (5-cm) piece of heat-shrink tubing over the white lead of the twisted pair and solder the white lead to the emitter lead of Q3.
14. Slide the heat-shrink tubing over the exposed collector leads, emitter leads, and solder joints, and apply heat with a soldering iron to shrink.
15. With needlenose pliers, carefully bend the tab of Q3 back and forth until it breaks off.
16. Wrap the case of Q3 with one layer of insulating tape, making sure not to cover the glass lens on top.
17. Deburr the ends of the aluminum tube, both inside and out.
18. Slip the uncommitted end of the shielded, twisted pair through the aluminum tube, and slide the tube down to Q3. Carefully direct the shield and insulated leads of Q3 into the tube, and pull gently until Q3 is inset approximately 1 in (4 cm) into the tube. If Q3 does not slide easily into the tube, apply a small amount of lightweight lubricant to the tape surrounding Q3 before drawing it into the tube.

Note

The case of Q3 is common to the collector. Ensure that the insulating tape does not become dislodged when drawing Q3 into the tube, as the collector will have +5 V dc on it and the case will be grounded by contact with the shield. Failure to properly insulate Q3 could result in the failure of U127 in the power supply.

19. Cut the shielded, twisted pair to the appropriate length for use with the system. Strip the insulation, and solder the red lead to pin 22, the white lead to Z, and the shield to pin 21 of the 44-pin edge connector to be used on VIDEO-1 connector J1 (not supplied in the kits) after first slipping the heat-shrink tubing over the leads and shielding.

20. Connect the AIM-65 and VIDEO-1 with interconnect cable. Connect the other connector (with light pen attached) to the VIDEO-1 at J1.
    a. Measure the resistance between J1, pins 22, Z, and 21, to verify that no shorts exist.
    b. Apply both +5 V dc and +24 V dc to the system.
    c. Initialize BASIC, and enter the following program:

```
 10    POKE 40959, 0
 20    Z = PEEK (40957)
 30    A = PEEK (40958)
 40    POKE ((Z*256) + A-9), 32
 50    FOR X = 0 TO 100
 60    NEXT
 70    POKE ((Z*256) + A-9), 160
 80    GOTO 20
100    FOR X = 0 TO 512
110    POKE 32768 + X, 160
120    NEXT
```

    d. Turn on the television or monitor and RUN 100. The video display will switch to alphanumerics mode and fill the screen with white before the AIM will respond "FC error in 120."
    e. Now RUN 10. Hold the light pen against the screen, and adjust R10 until a black block appears near the location of the light pen. If a random block occurs as the program is running, the light pen may be responding to ambient light. R10 may be turned to adjust the sensitivity.

       Some experimentation with the setting of R10 versus the distance that Q3 is inset into the light pen tube will be required to attain optimum performance.

Note

The program listed in step c, above, may not accurately calculate the propagation and processing delays in the system, and, as a result, the bar will not necessarily appear at the exact position in which the light pen is being held. Refer to the software listing for a more accurate light pen program.

    f. If BASIC is not available, refer to the software assembly listing, and utilize the light pen portion of the program to verify light pen operation; make the appropriate adjustment of R10.
    g. If any problems occur in the performance of steps a through f, above, refer to the troubleshooting paragraph, Light Pen.

4.3.5.7 Final Assembly

The Final Assembly step on the VIDEO-1 is the cleaning of the rosin from the rear of the circuit board.

Use alcohol and a soft brush to remove the residue rosin.

CAUTION

DO NOT ALLOW ANY ALCOHOL TO CONTACT THE DISPLAYS ON THE AIM-65! ALCOHOL WILL CAUSE THE DISPLAYS TO CLOUD OR PARTIALLY DISSOLVE.

Refer to the VIDEO-1 Outline and Mounting Drawing (figure 9-6).

The VIDEO-1 has been designed to fit in a variety of cases and was shaped specifically to mount beneath the AIM-65 in either the standard case supplied by Rockwell or the case designed and distributed by the Cedar Valley Computer Association (formerly the Cedar Rapids AIM User's Group).

5.1 MOUNTING THE VIDEO-1 IN THE ROCKWELL CASE

In order to mount the VIDEO-1 in the Rockwell-supplied case, the 0.25-inch stand-offs must be removed and replaced by small washers (not supplied) stacked tall enough to keep the component leads from being bent on the bottom of the case.

The dimensions provided on the VIDEO-1 Outline and Mounting Drawing should be used to cut slots in the rear of the bottom of the case for connectors J1 and J3 clearance. Once the proper-size connector slots have been cut, the VIDEO-1 may be set into the bottom of the case to check for proper fit.

Remove the VIDEO-1 from the case and cut or drill a 0.25-inch-diameter hole in the case, centered between the slots cut for J1 and J3. Mount RF connector J2 in this hole.

Cut or drill seven 0.125-inch mounting holes in the bottom of the case according to the dimensions provided on the VIDEO-1 Outline and Mounting Drawing. Mount the VIDEO-1 by inserting the mounting screws through from the bottom of the case; install the washers on the screws; fit the VIDEO-1 over the screws; and secure the VIDEO-1 by utilizing the stand-offs as nuts on the top of the circuit board.

Connect J2 to the VIDEO-1, using 75-ohm subminiature coaxial cable as described in the Video Assembly paragraph, with the only difference being that the shield of the coaxial cable should be soldered to the J2 ground lug and the bracket mounting hole on the VIDEO-1.

5.2 MOUNTING THE VIDEO-1 IN THE C.R.A.U.G. CASE

Using the dimensions provided on the VIDEO-1 Outline and Mounting Drawing, cut two slots in the rear of the bottom of the case for J1 and J3, centered 0.25 inch above the bottom of the case.

A 0.5-inch hole should be cut or drilled in the rear center of the case, 1.0 inch above the bottom of the case, for J2.

Drill six 0.125-inch holes in the bottom of the case for mounting the VIDEO-1. (The center hole in the VIDEO-1 corresponds to the center mounting foot in the case and will not be used for mounting.)

Secure the VIDEO-1 by inserting six 0.19-inch-long 4-40 screws (not provided) through from the bottom of the case and screwing them into the threaded stand-offs on the VIDEO-1.

A majority of the potential faults on the VIDEO-1 may be isolated without special test equipment by properly observing the fault indications present. Rather than provide a technically oriented troubleshooting section, the author has opted to describe a method for general faultfinding that requires a minimum of test equipment.

Any fault on the VIDEO-1 may be immediately isolated by its fault indications into one of the following four categories:

1. Both the AIM-65 and VIDEO-1 are inoperative.
2. The AIM-65 operates normally, but the VIDEO-1 is inoperative.
3. One or more of the VIDEO-1 functional sections is inoperative.
4. One or more of the VIDEO-1 functional sections is intermittent.

Each of the above categories may be further broken down into circuit areas where it is probable that the fault is hiding. The following paragraphs suggest circuit areas for each category.

6.1 BOTH AIM-65 AND VIDEO-1 INOPERATIVE

Because each interconnect line between the AIM-65 and VIDEO-1 is buffered or isolated by a data transceiver, a limited number of potential faults exist. To isolate the fault area:

1. Verify that the +5-V dc bus on the VIDEO-1 is between +4.8 and +5.2 V dc. Voltages outside this range can cause erratic operation. If the +5 V dc is being pulled down, disconnect +5 V dc from the VIDEO-1, and power up the system. If the AIM-65 powers up normally without +5 V dc to the VIDEO-1, there are three possible problems:

   a. The power supply is not capable of providing sufficient amperage to drive the enlarged system (or it requires adjustment).
   b. A faulty component is shorting the +5 V dc to ground. If this is the case, the faulty component will typically become much hotter than the other components with power applied.
   c. A circuit short exists between +5 V dc and ground. The most likely shorts of this type would be between bypass capacitor leads.

2. If the AIM-65 fails to operate without power applied to the VIDEO-1, the fault is most likely either a short in the interconnect cable (or circuit traces) or failure of one of the buffers or data transceivers that isolate the VIDEO-1 from the AIM-65.

   The possibility of a short in either the interconnect cable or the circuit traces associated with edge connector J3 may be tested using an ohmmeter and checking for low-resistance readings between J3 connections with the interconnect cable attached.

The following is a listing of the VIDEO-1 components associated with the various signal lines from the AIM-65 expansion connector:

J3 PIN	SIGNAL	VIDEO-1 COMPONENTS
8	D7	U2, U112, U116, U117
9	D6	U2, U112, U116, U117
10	D5	U2, U112, U116, U117
11	D4	U2, U112, U116, U117
12	D3	U2, U112, U116, U117
13	D2	U2, U112, U116, U117
14	D1	U2, U112, U116, U117
15	D0	U2, U112, U116, U117
A	A0	U3, U86
B	A1	U3, U86
C	A2	U3, U86
D	A3	U3, U86
E	A4	U3, U86
F	A5	U3, U86
H	A6	U3, U86
J	A7	U3, U86
K	A8	U4, U85
L	A9	U4, U85
M	A10	U4, U85
N	A11	U4, U85
P	A12	U4, U85
R	A13	U85
S	A14	U85
T	A15	U85
U	Phase 2 clock	U7, U10, U87, U90, U118, U121
V	Syst $R/\overline{W}$	U3, U103
W	$R/\overline{W}$	U2, U10, U112, U116, U117, U120

Any J3 pins not in the above list are not used by the VIDEO-1 and terminate at a plated-through hole next to J3. If a short or low-resistance reading is encountered at J3, refer to the above list, determine the component(s) in common with the problem pins, remove those components, and again apply power. If the AIM-65 still fails to power up normally, the fault is probably a short between the circuit traces that run from J3 to the removed component locations.

6.2 AIM-65 OPERATES NORMALLY, BUT VIDEO-1 INOPERATIVE

A very limited number of faults can occur which can cause all of the various functional areas on the VIDEO-1 to be inoperative. On a fully populated VIDEO-1, there is no component common to all functional sections. The highest probability for a fault of this type would be an open circuit in the interconnect cable or in the traces from J3 to the various components listed in paragraph 6.1.

The use of an oscilloscope is the best method of locating open circuits on the VIDEO-1.

6.3 ONE OR MORE FUNCTIONAL CIRCUITS INOPERATIVE

If more than one functional circuit is inoperative, isolate the components that the circuits have in common, using the schematics.

If no oscilloscope is available, systematically replace the common components until the fault is corrected. This procedure is not as bad as it seems; the modular concepts incorporated in the VIDEO-1 minimize the number of common components between functional circuits.

If an oscilloscope is available, it may be synchronized with the phase 2 clock to capture any signal present on the VIDEO-1. As a general rule, chip selects and data lines will be valid during only the positive portion of phase 2.

To troubleshoot a given functional circuit, utilize the AIM-65 in a short loop to exercise the faulty circuit, while observing the questionable signal lines. As an example, if D/A No. 1 was not operable, it could be exercised by the following program:

```
0000   INY
0001   STY   9FFA
0004   JMP   0000
```

This program would generate a recurring ramp at about a 2-kHz rate with 256 steps per ramp. The outputs of U105 would be square waves that halved in frequency as outputs Q0 to Q7 were observed. With this program running, it would therefore be possible to trace the signals through D/A No. 1 in much the same way as one would trace through an all-analog circuit.

Similar test loops can be written to exercise any portion of the VIDEO-1 except the power supply. It is recommended that all test programs be written in machine code or assembly language due to the relatively long periods required by the AIM-65 to interpret BASIC. (The BASIC program, equivalent to the machine code program listed above, generates a 0.25-Hz ramp.)

In some cases, one circuit may be used to test another. For example, if the A/D is inoperable, D/A No. 2 can be used to provide a controlled input by the following program:

```
0000   LDA   #00   }
0002   STA   9FFC   }   Enables D/A No. 2 as offset for A/D.

0005   INY         }
0006   STY   9FFB   }   Generates ramp from D/A No. 2.

0009   LDA   9FFC   }   Starts A/D conversion.

000C   JMP   0005   }   Loops.
```

This program utilizes a bipolar ramp from D/A No. 2 as an input to the A/D converter through the noninverting input of U131. The inputs to comparator U89B may then be compared to see if they track each other and generate a pulse width modulated signal from the comparator. The outputs of SAR U100 may also be observed to ensure that they switch, and $\overline{CC}$ should pulse 256 times per ramp.

The above programs are examples only; use your imagination and make use of the AIM-65 wherever possible to simplify circuit testing.

6.4 FUNCTIONAL SECTION(S) INTERMITTENT

Intermittent faults may be caused by a variety of different problems, including cold solder joints, unsoldered pins, cracked traces, insufficient current or wrong voltages from the

power supply, borderline timing problems, etc. As a result, intermittent faults are the most difficult to track down.

In troubleshooting an intermittent fault, first eliminate the obvious; check the voltages on the power bus in the suspect area. If the voltage on the +5 V dc is less than 4.9 V or greater than 5.1 V, adjust the power supply to correct. Examine the solder joints in the suspect area. Resolder any questionable connection. Visually inspect the traces in the suspect area. If a trace has a suspected crack, measure the resistance of the trace while gently flexing the circuit board.

Note

While building the final production prototypes of the VIDEO-1, it was observed that the 2114 RAM's were particularly critical of the +5-V dc bus level. With some 2114 IC's ±0.2 V on the +5-V bus was sufficient to cause intermittent operation.

Once the obvious checks have been done, testing becomes a bit more complicated. Intermittent RAM may be isolated by utilizing the memory test listed in appendix VII. To verify whether the RAM or its associated signal lines and chip select are at fault, swap the suspect RAM with a RAM from a location which tests as good, and test both the suspect location and the location the suspect RAM now occupies.

If timing problems are suspected, a dual-trace oscilloscope will be required to perform the testing. Refer to the AIM-65 Hardware Manual for the 6502 timing diagrams. With one channel of the oscilloscope, observe the phase 2 clock. With the other channel, observe the chip selects, latch clock inputs, etc, to ensure that the VIDEO-1 signal lines transition within the tolerances specified in the AIM-65 Hardware Manual. If a timing discrepancy exists, trace back toward the AIM-65 until the timing is within tolerance to isolate the faulty stage. To best observe the timing, utilize looped programs generated by the AIM-65 similar to the examples shown in paragraph 6.3.

Be creative in your use of the AIM-65 during testing. Set up test programs that exercise the intermittent circuit in a simulation of the conditions when the intermittent fault most often occurs. The better the simulation, the easier it will be to isolate the problem.

The VIDEO-1 design was intended to provide maximum flexibility as an interface between the AIM-65 and the outside world. Actual usage of the VIDEO-1 will, of course, be dependent on the requirements of each individual.

For those individuals that now own a VIDEO-1 but are at a loss as to what to do with it, the following is a list of applications that are theoretically possible with the appropriate software:

1. Audio modification/enhancement (ie, reverberation, echo, filtering, pseudostereo from monaural sources, digital signal mixing, etc).
2. Audio generation (ie, voice or music synthesis, FSK or tone generation, etc).
3. Audio recognition (ie, processor control via voice or sound, FSK decoding, etc).
4. Visual presentation of audio signals (ie, oscillography, spectral and network analysis, color organ, music notation, etc).
5. Visual presentation of digital data (ie, artwork generation, animation, memory testing, etc).

The above list is but a sampling of the practical applications of the VIDEO-1. Details of each application's software implementation would require a separate book and are outside the scope of this manual.

The Cedar Valley Computer Association's monthly news letter, Interchange, is the recommended vehicle for exchanging software and circuit ideas that utilize the VIDEO-1.

Submittals to, or questions regarding, the Interchange should be sent to:

Cedar Valley Computer Association
Post Office Box 671
Marion, Iowa 52302
Attention: Editor, Interchange

To get started in visual display manipulation, the following BASIC subroutings are worthwhile learning tools and may be utilized in expanded user programs:

```
10 E=1
20 Y3=INT[192*RND[1]]
30 X3=INT[256*RND[1]]
40 Y=INT[192*RND[1]]
50 X=INT[256*RND[1]]
55 PRINT X, Y
60 GOSUB 9200
70 GOTO 40
100 INPUT X3 Y3
105 E=1
110 INPUT X, Y
120 GOSUB 9200
130 GOTO 100
200 E=1
210 Y3=0
220 X3=128
230 Y=191
240 X=128
250 GOSUB 9200
260 X3=0
270 Y3=95
280 X=255
290 Y=95
300 GOSUB 9200
310 RETURN
400 E=1
410 GOSUB 200
420 D0= 052359878
430 FOR  G=1TO0STEP-1
440 X3=234
450 Y3=95
460 FOR D1=1TO120
470 X=80*COS[D0*D1]*4/3+128
480 Y=80*SIN[D0*D1]*G+95
490 GOSUB 9200
500 NEXT
510 NEXT
520 END
600 E=1
610 INPUT DF
620 INPUT TT
630 TL=0
635 GOSUB 200
640 X=80*COS[TL*TT*DF]*4/3+128
650 Y=80*SIN[TL*TT]+95
660 IF TL=0 THEN X3=X
670 IF TL=0 THEN Y3=Y
680 GOSUB 9200
690 TL=TL+1
700 GOTO 640
9000 X5=X
9010 Y5=Y
9020 X0=INT[X5]
9030 Y0=INT[Y5]
9040 IF X0>255 OR Y0>191 GOTO 9130
9045 IF X0<0 OR Y0<0 GOTO 9130
9050 X1=INT[X0/8]
9060 T=38880-Y0*32+X1
9070 T1=PEEK[T]
9080 X2=INT[2↑[7-INT[8*[X0/8-X1]]]]
9090 T2=T1ANDX2
9100 IF T2=X2 THEN T1=T1-X2
9110 T1=T1+E*X2
9120 POKE T, T1
9130 RETURN
9200 Y4=INT[Y]
9210 X4=INT[X]
9220 N0=Y4-Y3
9230 N1=X4-X3
9240 M=10000
9250 IF N1<>0 THEN M=N0/N1
9260 B=Y4-M*X4
9270 IF ABS[M]>1 GOTO 9340
9280 S=SGN[N1]
9290 FOR X5=X3TOX4STEPS
9300 Y5=X5*M+B
9310 GOSUB 9020
9320 NEXT
9330 GOTO 9390
9340 S=SGN[N0]
9350 FOR Y5=Y3TOY4STEPS
9360 X5=[Y5-B]/M
9370 GOSUB 9020
9388 NEXT
9390 Y3=Y4
9400 X3=X4
9410 RETURN
9500 FOR X=0TO6144
9510 POKE 32768+X,0
9520 NEXT
9530 END
```

The above program contains several segments which run independently but utilize common subroutines.

RUN 1Ø starts a random line generator.

RUN 1ØØ starts a program which draws a line between two specified points. At start-up, the program waits for the X, Y coordinates of point 2. These coordinates become X4, Y4. The line will be drawn from point 1 to point 2, point 1 being coordinates Ø,Ø (lower left corner of display) unless otherwise specified. At the end of this program, point 2 becomes point 1, and the program then waits for another set of point 2 X,Y coordinates.

RUN 2ØØ starts a program which draws centered quadrant lines on the screen.

RUN 4ØØ starts a program which generates a family of elipses.

RUN 6ØØ starts a program which generates Lissajous patterns given: DF as the difference in frequency and TT as the time delta.

RUN 95ØØ starts a program which will clear the screen in maximum graphics.

The subroutine starting at 9200 is the draw line subroutine utilized by the above programs to connect the points specified in the program.

In order to utilize the above programs, first:

POKE 40959, 255

to place the VIDEO-1 in maximum graphics. If maximum color graphics is preferred, use:

POKE 40959, 254.

8.1 ALPHANUMERIC COMPONENT LISTING

REF DESIG	VENDOR P/N	CPN	DESCRIPTION
C1		913-3279-200	Capacitor, 0.1μF, ceramic
C2		913-1098-020	Capacitor, 47pF, NPO
C3		913-3279-200	Capacitor, 0.1μF, ceramic
C4		913-3279-200	Capacitor, 0.1μF, ceramic
C5		913-4003-000	Capacitor, 56pF, mica
C6		917-1225-000	Capacitor, 9-35pF, trimmer
C7		913-3281-320	Capacitor, 0.01μF, NPO
C8		913-3279-200	Capacitor, 0.1μF, ceramic
C9		913-3279-200	Capacitor, 0.1μF, ceramic
C10		913-3279-200	Capacitor, 0.1μF, ceramic
C11		913-3279-200	Capacitor, 0.1μF, ceramic
C12		913-3279-200	Capacitor, 0.1μF, ceramic
C13		913-3279-200	Capacitor, 0.1μF, ceramic
C14		913-3279-200	Capacitor, 0.1μF, ceramic
C15		913-3279-200	Capacitor, 0.1μF, ceramic
C16		913-3279-200	Capacitor, 0.1μF, ceramic
C17		913-3279-200	Capacitor, 0.1μF, ceramic
C18		913-3279-200	Capacitor, 0.1μF, ceramic
C19		913-3279-200	Capacitor, 0.1μF, ceramic
C20		913-3279-200	Capacitor, 0.1μF, ceramic
C21		913-3279-200	Capacitor, 0.1μF, ceramic
C22		913-3279-200	Capacitor, 0.1μF, ceramic
C23		913-3279-200	Capacitor, 0.1μF, ceramic
C24		913-3279-200	Capacitor, 0.1μF, ceramic
C25		913-3279-200	Capacitor, 0.1μF, ceramic
C26		913-3279-200	Capacitor, 0.1μF, ceramic
C27		913-3279-200	Capacitor, 0.1μF, ceramic
C28		913-3279-200	Capacitor, 0.1μF, ceramic
C29		913-3279-200	Capacitor, 0.1μF, ceramic
C30		913-3279-200	Capacitor, 0.1μF, ceramic
C31		913-3279-200	Capacitor, 0.1μF, ceramic
C32		913-3279-200	Capacitor, 0.1μF, ceramic
C33		913-3279-200	Capacitor, 0.1μF, ceramic
C34		913-3279-200	Capacitor, 0.1μF, ceramic
C35		913-3279-200	Capacitor, 0.1μF, ceramic
C36		913-3279-200	Capacitor, 0.1μF, ceramic
C37		913-3279-200	Capacitor, 0.1μF, ceramic
C38		913-3279-200	Capacitor, 0.1μF, ceramic
C39		913-3279-200	Capacitor, 0.1μF, ceramic
C40		913-3279-200	Capacitor, 0.1μF, ceramic
C41		913-3279-200	Capacitor, 0.1μF, ceramic
C42		913-3279-200	Capacitor, 0.1μF, ceramic
C43		913-3279-200	Capacitor, 0.1μF, ceramic
C44		913-3279-200	Capacitor, 0.1μF, ceramic
C45		913-3279-200	Capacitor, 0.1μF, ceramic
C46		913-3279-200	Capacitor, 0.1μF, ceramic
C47		913-3279-200	Capacitor, 0.1μF, ceramic
C48		913-3279-200	Capacitor, 0.1μF, ceramic
C49		913-3279-200	Capacitor, 0.1μF, ceramic
C50		913-3279-200	Capacitor, 0.1μF, ceramic
C51		913-3279-200	Capacitor, 0.1μF, ceramic

REF DESIG	VENDOR P/N	CPN	DESCRIPTION
C52		913-3279-200	Capacitor, 0.1μF, ceramic
C53		913-3279-200	Capacitor, 0.1μF, ceramic
C54		913-3279-200	Capacitor, 0.1μF, ceramic
C55		913-3279-200	Capacitor, 0.1μF, ceramic
C56		913-3279-200	Capacitor, 0.1μF, ceramic
C57		913-3279-200	Capacitor, 0.1μF, ceramic
C58		913-3279-200	Capacitor, 0.1μF, ceramic
C59		913-3279-200	Capacitor, 0.1μF, ceramic
C60		913-3279-200	Capacitor, 0.1μF, ceramic
C61		913-3279-200	Capacitor, 0.1μF, ceramic
C62		913-3279-200	Capacitor, 0.1μF, ceramic
C63		913-3279-200	Capacitor, 0.1μF, ceramic
C64		913-3279-200	Capacitor, 0.1μF, ceramic
C65		913-3279-200	Capacitor, 0.1μF, ceramic
C66		184-9102-890	Capacitor, 47μF, 35V, tantalum
C67		184-9102-190	Capacitor, 47μF, 20V, tantalum
C68		184-9102-170	Capacitor, 10μF, 20V, tantalum
C69		913-3279-200	Capacitor, 0.1μF, ceramic
C70		913-3279-110	Capacitor, 0.01μF, ceramic
C71		913-3279-110	Capacitor, 0.01μF, ceramic
C72		184-9086-490	Capacitor, 15μF, 20V, tantalum
C73		184-9102-170	Capacitor, 10μF, 20V, tantalum
C74		184-9102-170	Capacitor, 10μF, 20V, tantalum
C75		913-3279-200	Capacitor, 0.1μF, ceramic
C76		912-4141-130	Capacitor, 15pF, mica
C77		913-3279-200	Capacitor, 0.1μF, ceramic
C78		913-3279-200	Capacitor, 0.1μF, ceramic
C79		912-4141-330	Capacitor, 68pF, mica
C80		913-3279-200	Capacitor, 0.1μF, ceramic
C81		913-3279-200	Capacitor, 0.1μF, ceramic
C82		913-3279-200	Capacitor, 0.1μF, ceramic
C83		912-4141-130	Capacitor, 15pF, mica
C84		913-3279-200	Capacitor, 0.1μF, ceramic
C85		913-3279-200	Capacitor, 0.1μF, ceramic
C86		912-4141-330	Capacitor, 68pF, mica
C87		913-3279-200	Capacitor, 0.1μF, ceramic
C88		913-3279-200	Capacitor, 0.1μF, ceramic
C89		913-3279-200	Capacitor, 0.1μF, ceramic
C90		913-3279-200	Capacitor, 0.1μF, ceramic
C91		913-3279-200	Capacitor, 0.1μF, ceramic
C92		912-4141-130	Capacitor, 15pF, mica
C93		913-3279-200	Capacitor, 0.1μF, ceramic
C94		913-3279-200	Capacitor, 0.1μF, ceramic
C95		912-4141-330	Capacitor, 68pF, mica
C96		913-3279-200	Capacitor, 0.1μF, ceramic
C97		913-3279-200	Capacitor, 0.1μF, ceramic
C98		912-4141-350	Capacitor, 82pF, mica
C99		913-3279-200	Capacitor, 0.1μF, ceramic
C100		913-3279-200	Capacitor, 0.1μF, ceramic
C101		913-3279-200	Capacitor, 0.1μF, ceramic
C102		913-3279-200	Capacitor, 0.1μF, ceramic
C103		913-3279-200	Capacitor, 0.1μF, ceramic
C104		913-3279-200	Capacitor, 0.1μF, ceramic
C105		913-3279-200	Capacitor, 0.1μF, ceramic
C106		913-3279-200	Capacitor, 0.1μF, ceramic
C107		913-3279-200	Capacitor, 0.1μF, ceramic
C108		913-3279-200	Capacitor, 0.1μF, ceramic
C109		913-3279-200	Capacitor, 0.1μF, ceramic
C110		913-3279-200	Capacitor, 0.1μF, ceramic
C111		913-3279-200	Capacitor, 0.1μF, ceramic
C112		913-3279-200	Capacitor, 0.1μF, ceramic
C113		913-3279-200	Capacitor, 0.1μF, ceramic

REF DESIG	VENDOR P/N	CPN	DESCRIPTION
C114		913-3279-200	Capacitor, 0.1μF, ceramic
C115		913-3279-200	Capacitor, 0.1μF, ceramic
C116		913-3279-200	Capacitor, 0.1μF, ceramic
C117		913-3279-200	Capacitor, 0.1μF, ceramic
C118		913-3279-200	Capacitor, 0.1μF, ceramic
C119		913-3279-200	Capacitor, 0.1μF, ceramic
C120		913-3279-200	Capacitor, 0.1μF, ceramic
C121		913-3279-200	Capacitor, 0.1μF, ceramic
C122		913-3279-200	Capacitor, 0.1μF, ceramic
C123		913-3279-200	Capacitor, 0.1μF, ceramic
C124		913-3279-200	Capacitor, 0.1μF, ceramic
C125		913-3279-200	Capacitor, 0.1μF, ceramic
C126		913-3279-200	Capacitor, 0.1μF, ceramic
C127		913-3279-200	Capacitor, 0.1μF, ceramic
C128		913-3279-200	Capacitor, 0.1μF, ceramic
C129		913-3279-200	Capacitor, 0.1μF, ceramic
C130		913-3279-200	Capacitor, 0.1μF, ceramic
C131		913-3279-200	Capacitor, 0.1μF, ceramic
C132		913-3279-200	Capacitor, 0.1μF, ceramic
C133		913-3279-200	Capacitor, 0.1μF, ceramic
C134		913-3279-200	Capacitor, 0.1μF, ceramic
C135		913-3281-270	Capacitor, 0.001μF, NPO
CR1	IN5415	353-6558-010	Diode
CR2	IN5415	353-6558-010	Diode
CR3	IN5415	353-6558-010	Diode
J2	3501FP		Phono jack, RCA, switchcraft
L1		242-0447-220	Coil, 0.1μH, adjustable, aluminum slug
L2		240-2715-010	Coil, 0.1μH, rf shielded
Q1	2N2222A	352-0661-020	Transistor, NPN
Q2	2N2907A	352-0551-010	Transistor, PNP
Q3	MRD370	128-0076-004	Transistor, photo-Darlington
R1		745-0748-000	Resistor, 1kΩ, 1/4W, 5%
R2		745-0759-000	Resistor, 2kΩ, 1/4W, 5%
R3		745-0775-000	Resistor, 5.6kΩ, 1/4W, 5%
R4		745-0744-000	Resistor, 750Ω, 1/4W, 5%
R5		745-0708-000	Resistor, 75Ω, 1/4W, 5%
R6		745-0726-000	Resistor, 240Ω, 1/4W, 5%
R7		745-0726-000	Resistor, 240Ω, 1/4W, 5%
R8		382-0012-290	Resistor, 10kΩ, trimmer
R9		745-1863-490	Resistor, 1kΩ, 1/8W, 5%
R10		382-0012-290	Resistor, 10kΩ, trimmer
R11		745-1863-250	Resistor, 100Ω, 1/8W, 5%
R12		745-1863-250	Resistor, 100Ω, 1/8W, 5%
R13		745-1863-340	Resistor, 240Ω 1/8W, 5%
R14		382-0012-280	Resistor, 5kΩ, trimmer
R15		745-1863-560	Resistor, 2kΩ, 1/8W, 5%
R16		747-2178-970	Resistor, 45.3Ω, 1W, 1%
R17		745-1863-560	Resistor, 2kΩ, 1/8W, 5%
R18			
R19		745-1863-270	Resistor, 120Ω, 1/8W, 5%
R20		382-0012-270	Resistor, 2kΩ, trimmer
R21		382-0012-280	Resistor, 5kΩ, trimmer

REF DESIG	VENDOR P/N	CPN	DESCRIPTION
R22		745-1863-600	Resistor, 3kΩ, 1/8W, 5%
R23		745-1863-600	Resistor, 3kΩ, 1/8W, 5%
R24		745-1863-600	Resistor, 3kΩ, 1/8W, 5%
R25		382-0012-280	Resistor, 5kΩ, trimmer
R26		382-0012-290	Resistor, 10kΩ, trimmer
R27		745-1863-170	Resistor, 47Ω, 1/8W, 5%
R28		745-1863-600	Resistor, 3kΩ, 1/8W, 5%
R29		745-1863-600	Resistor, 3kΩ, 1/8W, 5%
R30		745-1863-600	Resistor, 3kΩ, 1/8W, 5%
R31		382-0012-280	Resistor, 5kΩ, trimmer
R32		382-0012-290	Resistor, 10kΩ, trimmer
R33		745-1863-600	Resistor, 3kΩ, 1/8W, 5%
R34		745-1863-600	Resistor, 3kΩ, 1/8W, 5%
R35		745-1863-600	Resistor, 3kΩ, 1/8W, 5%
R36		745-1863-830	Resistor, 27kΩ, 1/8W, 5%
R37		382-0012-330	Resistor, 100kΩ, trimmer
R38		745-1863-650	Resistor, 4.7kΩ, 1/8W, 5%
R39		745-1863-730	Resistor, 10kΩ, 1/8W, 5%
R40		745-1863-730	Resistor, 10kΩ, 1/8W, 5%
R41		745-1863-490	Resistor, 1kΩ, 1/8W, 5%
R42		350-4030-150	Resistor, 1MΩ, network, dip
R43		350-4030-150	Resistor, 1MΩ, network, dip
R44		350-4030-150	Resistor, 1MΩ, network, dip
R45		745-1863-530	Resistor, 1.5kΩ, 1/8W, 5%
R46		745-1863-580	Resistor, 2.4kΩ, 1/8W, 5%
R47		745-1863-650	Resistor, 4.7kΩ, 1/8W, 5%
R48		745-1863-730	Resistor, 10kΩ, 1/8W, 5%
R49		745-1863-860	Resistor, 36kΩ, 1/8W, 5%
R50		745-1864-050	Resistor, 150kΩ, 1/8W, 5%
R51		745-1864-120	Resistor, 300kΩ, 1/8W, 5%
R52		382-0012-370	Resistor, 1MΩ, trimmer
R53		382-0012-300	Resistor, 20kΩ, trimmer
R54		745-1863-530	Resistor, 1.5kΩ, 1/8W, 5%
R55		745-1863-650	Resistor, 4.7kΩ, 1/8W, 5%
R56		745-1863-080	Resistor, 20Ω, 1/8W, 5%
R57		745-1863-080	Resistor, 20Ω, 1/8W, 5%
R58		745-1863-170	Resistor, 47Ω, 1/8W, 5%
R59		745-1863-170	Resistor, 47Ω, 1/8W, 5%
R60		745-1863-170	Resistor, 47Ω, 1/8W, 5%
R61		745-1863-170	Resistor, 47Ω, 1/8W, 5%
R62		745-1863-170	Resistor, 47Ω, 1/8W, 5%
R63		745-1863-170	Resistor, 47Ω, 1/8W, 5%
R64		745-1863-170	Resistor, 47Ω, 1/8W, 5%
R65		745-1863-170	Resistor, 47Ω, 1/8W, 5%
R66		745-1863-170	Resistor, 47Ω, 1/8W, 5%
R67		745-1863-530	Resistor, 1.5kΩ, 1/8W, 5%
TB1		367-1559-120	Block, terminal
U1	74LS374	351-1821-030	IC, 8-bit latch, T.S.
U2	74LS245	351-1849-020	IC, 8-bit data transceiver, T.S.
U3	74LS244	351-1841-030	IC, 8-bit buffer, T.S.
U4	74LS244	351-1841-030	IC, 8-bit buffer, T.S.
U5	74LS85	351-1697-010	IC, 4-bit comparator
U6	74LS42	351-1526-050	IC, 1-of-10 decoder
U7	74LS85	351-1697-010	IC, 4-bit comparator
U8	74LS85	351-1697-010	IC, 4-bit comparator
U9	74LS30	351-1523-140	IC, 8-input NAND
U10	74LS10	351-1523-230	IC, triple-3-input NAND
U11	MC6847	128-0076-001	IC, video display generator

REF DESIG	VENDOR P/N	CPN	DESCRIPTION
U12	MC1372	128-0076-002	IC, rf modulator
U13	2114 (L)	351-8413-030	IC, static memory 1Kx4
U14	2114 (L)	351-8413-030	IC, static memory 1Kx4
U15	2114 (L)	351-8413-030	IC, static memory 1Kx4
U16	2114 (L)	351-8413-030	IC, static memory 1Kx4
U17	2114 (L)	351-8413-030	IC, static memory 1Kx4
U18	2114 (L)	351-8413-030	IC, static memory 1Kx4
U19	2114 (L)	351-8413-030	IC, static memory 1Kx4
U20	2114 (L)	351-8413-030	IC, static memory 1Kx4
U21	2114 (L)	351-8413-030	IC, static memory 1Kx4
U22	2114 (L)	351-8413-030	IC, static memory 1Kx4
U23	2114 (L)	351-8413-030	IC, static memory 1Kx4
U24	2114 (L)	351-8413-030	IC, static memory 1Kx4
U25	74LS138	351-1526-030	IC, 1-of-8 decoder
U26	74LS138	351-1526-030	IC, 1-of-8 decoder
U27	2114 (L)	351-8413-030	IC, static memory, 1Kx4
U28	2114 (L)	351-8413-030	IC, static memory, 1Kx4
U29	2114 (L)	351-8413-030	IC, static memory, 1Kx4
U30	2114 (L)	351-8413-030	IC, static memory, 1Kx4
U31	2114 (L)	351-8413-030	IC, static memory, 1Kx4
U32	2114 (L)	351-8413-030	IC, static memory, 1Kx4
U33	2114 (L)	351-8413-030	IC, static memory, 1Kx4
U34	2114 (L)	351-8413-030	IC, static memory, 1Kx4
U35	2114 (L)	351-8413-030	IC, static memory, 1Kx4
U36	2114 (L)	351-8413-030	IC, static memory, 1Kx4
U37	2114 (L)	351-8413-030	IC, static memory, 1Kx4
U38	2114 (L)	351-8413-030	IC, static memory, 1Kx4
U39	2114 (L)	351-8413-030	IC, static memory, 1Kx4
U40	2114 (L)	351-8413-030	IC, static memory, 1Kx4
U41	2114 (L)	351-8413-030	IC, static memory, 1Kx4
U42	2114 (L)	351-8413-030	IC, static memory, 1Kx4
U43	2114 (L)	351-8413-030	IC, static memory, 1Kx4
U44	2114 (L)	351-8413-030	IC, static memory, 1Kx4
U45	2114 (L)	351-8413-030	IC, static memory, 1Kx4
U46	2114 (L)	351-8413-030	IC, static memory, 1Kx4
U47	2114 (L)	351-8413-030	IC, static memory, 1Kx4
U48	2114 (L)	351-8413-030	IC, static memory, 1Kx4
U49	2114 (L)	351-8413-030	IC, static memory, 1Kx4
U50	2114 (L)	351-8413-030	IC, static memory, 1Kx4
U51	2114 (L)	351-8413-030	IC, static memory, 1Kx4
U52	2114 (L)	351-8413-030	IC, static memory, 1Kx4
U53	2114 (L)	351-8413-030	IC, static memory, 1Kx4
U54	2114 (L)	351-8413-030	IC, static memory, 1Kx4
U55	2114 (L)	351-8413-030	IC, static memory, 1Kx4
U56	2114 (L)	351-8413-030	IC, static memory, 1Kx4
U57	2114 (L)	351-8413-030	IC, static memory, 1Kx4
U58	2114 (L)	351-8413-030	IC, static memory, 1Kx4
U59	2114 (L)	351-8413-030	IC, static memory, 1Kx4
U60	2114 (L)	351-8413-030	IC, static memory, 1Kx4
U61	2114 (L)	351-8413-030	IC, static memory, 1Kx4
U62	2114 (L)	351-8413-030	IC, static memory, 1Kx4
U63	2114 (L)	351-8413-030	IC, static memory, 1Kx4
U64	2114 (L)	351-8413-030	IC, static memory, 1Kx4
U65	2114 (L)	351-8413-030	IC, static memory, 1Kx4
U66	2114 (L)	351-8413-030	IC, static memory, 1Kx4
U67	2114 (L)	351-8413-030	IC, static memory, 1Kx4
U68	2114 (L)	351-8413-030	IC, static memory, 1Kx4
U69	2114 (L)	351-8413-030	IC, static memory, 1Kx4
U70	2114 (L)	351-8413-030	IC, static memory, 1Kx4
U71	2114 (L)	351-8413-030	IC, static memory, 1Kx4
U72	2114 (L)	351-8413-030	IC, static memory, 1Kx4
U73	2114 (L)	351-8413-030	IC, static memory, 1Kx4
U74	2114 (L)	351-8413-030	IC, static memory, 1Kx4

REF DESIG	VENDOR P/N	CPN	DESCRIPTION
U75	2114 (L)	351-8413-030	IC, static memory, 1Kx4
U76	2114 (L)	351-8413-030	IC, static memory, 1Kx4
U77	2114 (L)	351-8413-030	IC, static memory, 1Kx4
U78	2114 (L)	351-8413-030	IC, static memory, 1Kx4
U79	2114 (L)	351-8413-030	IC, static memory, 1Kx4
U80	2114 (L)	351-8413-030	IC, static memory, 1Kx4
U81	2114 (L)	351-8413-030	IC, static memory, 1Kx4
U82	2114 (L)	351-8413-030	IC, static memory, 1Kx4
U83	74LS138	351-1526-030	IC, 1-of-8 decoder
U84	74LS138	351-1526-030	IC, 1-of-8 decoder
U85	74LS244	351-1841-030	IC, 8-bit buffer, T.S.
U86	74LS244	351-1841-030	IC, 8-bit buffer, T.S.
U87	74LS00	351-1523-110	IC, quad-2-input NAND
U88	74LS244	351-1841-030	IC, 8-bit buffer, T.S.
U89	LM319N	351-1166-010	IC, dual comparator
U90	74LS112	351-1525-030	IC, dual J-K flip-flop
U91	74LS374	351-1821-030	IC, 8-bit latch, T.S.
U92	74LS374	351-1821-030	IC, 8-bit latch, T.S.
U93	4051	351-8236-010	IC, analog multiplexer
U94	LF356N	351-1287-040	IC, operational amplifier
U95	4051	351-8236-010	IC, analog multiplexer
U96	74LS374	351-1821-030	IC, 8-bit latch, T.S.
U97	LF356N	351-1287-040	IC, operational amplifier
U98	74LS02	351-1523-220	IC, quad-2-input NOR
U99	74LS00	351-1523-110	IC, quad-2-input NAND
U100	2502	128-0076-003	IC, successive approximation register
U101	1408	351-1152-010	IC, digital-to-analog converter
U102	74LS374	351-1821-030	IC, 8-bit latch, T.S.
U103	74LS244	351-1841-030	IC, 8-bit buffer, T.S.
U104	74LS374	351-1821-030	IC, 8-bit latch, T.S.
U105	74LS374	351-1821-030	IC, 8-bit latch, T.S.
U106	74LS374	351-1821-030	IC, 8-bit latch, T.S.
U107	1408	351-1152-010	IC, digital-to-analog converter
U108	1408	351-1152-010	IC, digital-to-analog converter
U109	LF356N	351-1287-040	IC, operational amplifier
U110	4051	351-8236-010	IC, analog multiplexer
U111	4051	351-8236-010	IC, analog multiplexer
U112	2716	351-8432-010	IC, μV eraseable PROM, 2Kx8
U113	74LS00	351-1523-110	IC, quad-2-input NAND
U114	LM340T-15	351-1120-050	Voltage regulator, +15V dc
U115	555	351-1137-020	IC, timer
U116	74LS245	351-1849-020	IC, 8-bit data transceiver, T.S.
U117	74LS245	351-1849-020	IC, 8-bit data transceiver, T.S.
U118	74LS138	351-1526-030	IC, 1-of-8 decoder
U119	74LS32	351-1523-260	IC, quad-2-input OR
U120	74LS02	351-1523-220	IC, quad-2-input NOR
U121	74LS00	351-1523-110	IC, quad-2-input NAND
U122	4053	351-8236-020	IC, CMOS analog switch
U123	74LS123	351-1699-020	IC, dual monostable multivibrator
U124	LM318	351-1153-040	IC, comparator, high speed
U125	LM317MP	128-0076-005	Voltage regulator
U126	LM337MP	128-0076-007	Voltage regulator
U127	LM340LAZ-5	128-0076-006	Voltage regulator
U128	LM340LAZ-5	128-0076-006	Voltage regulator
U129	LM320LZ-5	128-0076-008	Voltage regulator
U130	LF356N	351-1287-040	IC, operational amplifier
U131	LF346N	351-1287-040	IC, operational amplifier
Y1			3.579545-MHz crystal

REF DESIG	VENDOR P/N	CPN	DESCRIPTION
HARDWARE			
		763-7388-004	Bracket, mounting
		313-0132-000	Nut, hex, 4-40 (All)
		343-0133-000	Screw, panhead, 0.25 in, 4-40 (All)
		540-9033-003	Stand-off, 0.25 in, 4-40 (All)
		804-3084-022	Tubing, aluminum, 0.200 in I.D., 6 in long
		310-0779-030	Washer, 0.25 in O.D.
		439-0650-000	Wire, shielded, twisted pair, 6 ft long

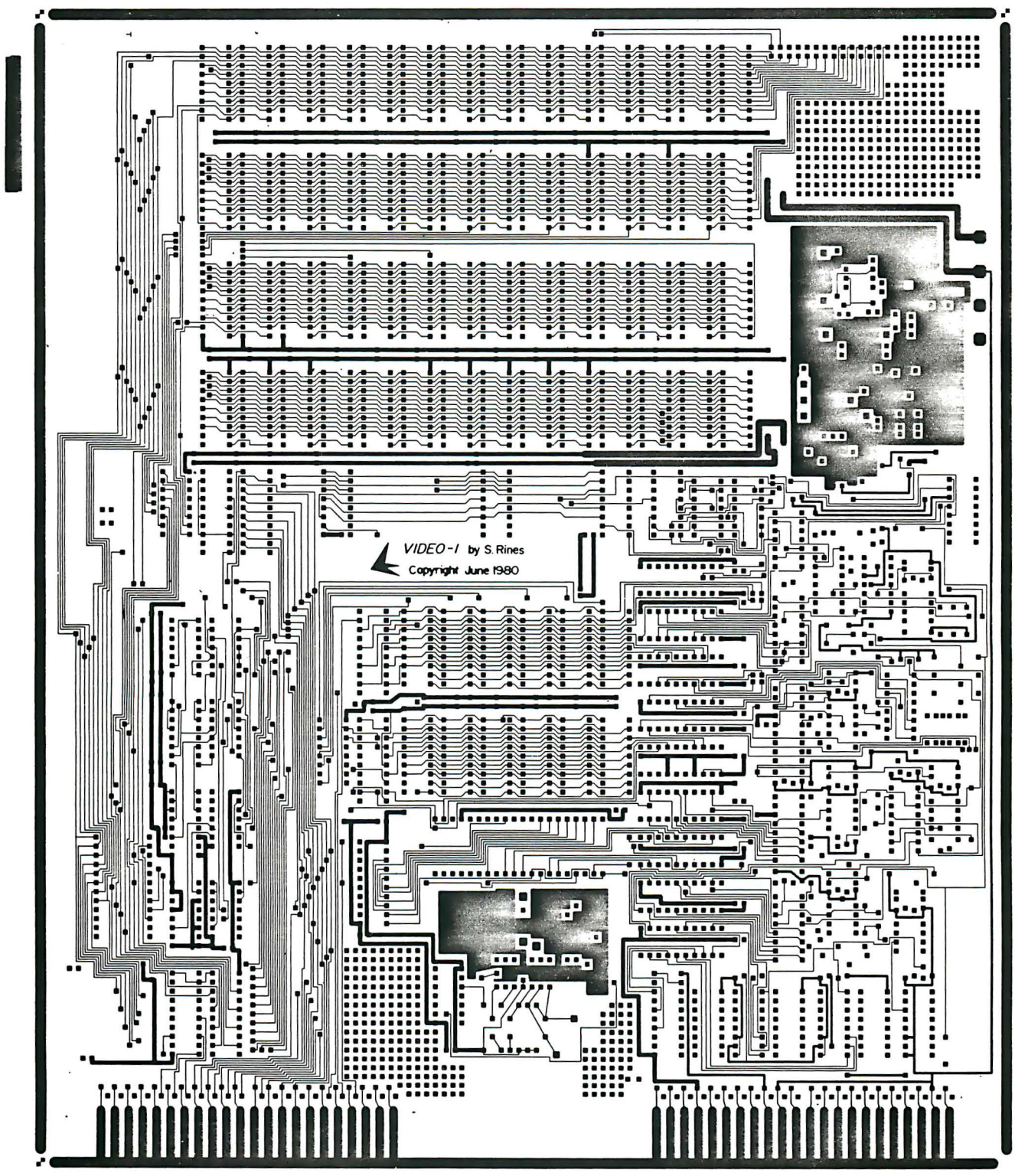


Figure 9-7. VIDEO-1 Top Layer Circuit Traces.

Appendixes

Seven appendixes follow. Appendixes I through IV are reprinted with permission of Motorola.

Appendix I

Motorola MOS VDG's

MOTOROLA
SEMICONDUCTORS
6501 ED BLUESTEIN BLVD., AUSTIN, TEXAS 78721

MC6847
NONINTERLACE
MC6847Y
INTERLACE

Advance Information

MOS
(N-CHANNEL, SILICON-GATE)

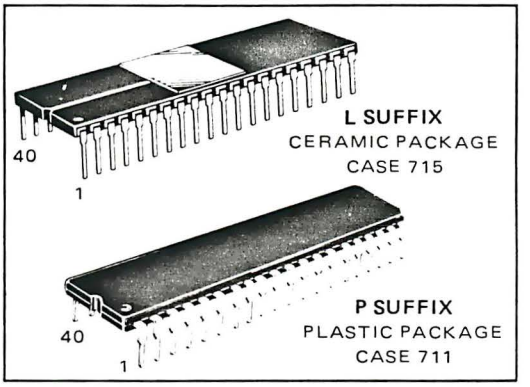
VIDEO
DISPLAY
GENERATOR

VIDEO DISPLAY GENERATOR (VDG)

The Motorola MC6847 Video Display Generator (VDG) provides a means of interfacing the Motorola M6800 microprocessor family (or similar products) to a commercially available color or black and white television receiver. Applications of the VDG include video games, bioengineering displays, education, communications and any place graphics are required.

The VDG reads data from memory and produces a composite video signal which will allow the generation of alphanumeric or graphic displays. The generated composite video may be up modulated to either Channel 3 or 4 by using the compatible MC1372 (TV Chroma and Video modulator). The up modulated signal is suitable for application to the antenna of a color TV. A typical TV game is indicated in Figure 1.

- Generates four different alphanumeric display modes and eight graphic display modes
- Compatible with the M6800 family
- Compatible with the MC1372 modulator
- The alphanumeric modes display 32 characters per line by 16 lines
- An internal multiplexer allows the use of either the internal ROM or an external character generator
- An external character generator can be used to extend the internal character set for "limited graphic" shapes
- A Mask Programmable internal character generator ROM is available on special order (Appendix A)
- One display mode offers 8-color 64 x 32 density graphics in an alphanumeric display mode
- One display mode offers 4-color 64 x 48 density graphics in an alphanumeric display mode
- All alphanumeric modes have a selectable video inverse
- Generates full video signal
- Generates R-Y and B-Y signals for external color modulator
- Full-graphic modes offer 64 x 64, 128 x 64, 128 x 96, 128 x 192, or 256 x 192 densities
- Full-graphic modes allow 2-color or 4-color data structures
- Full-graphic modes use one of two 4-color sets or one of two 2-color sets
- Available in either an interlace mode (NTSC Standard) or a non-interlace mode



PIN ASSIGNMENT

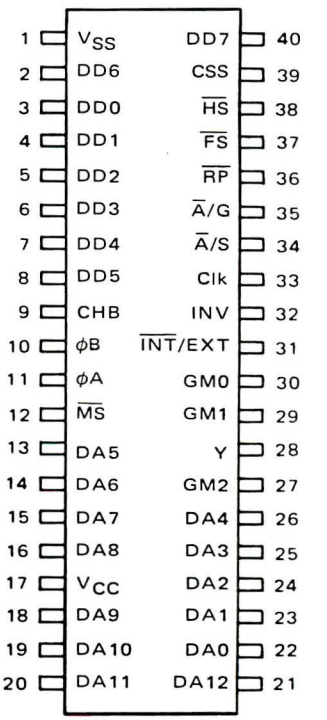
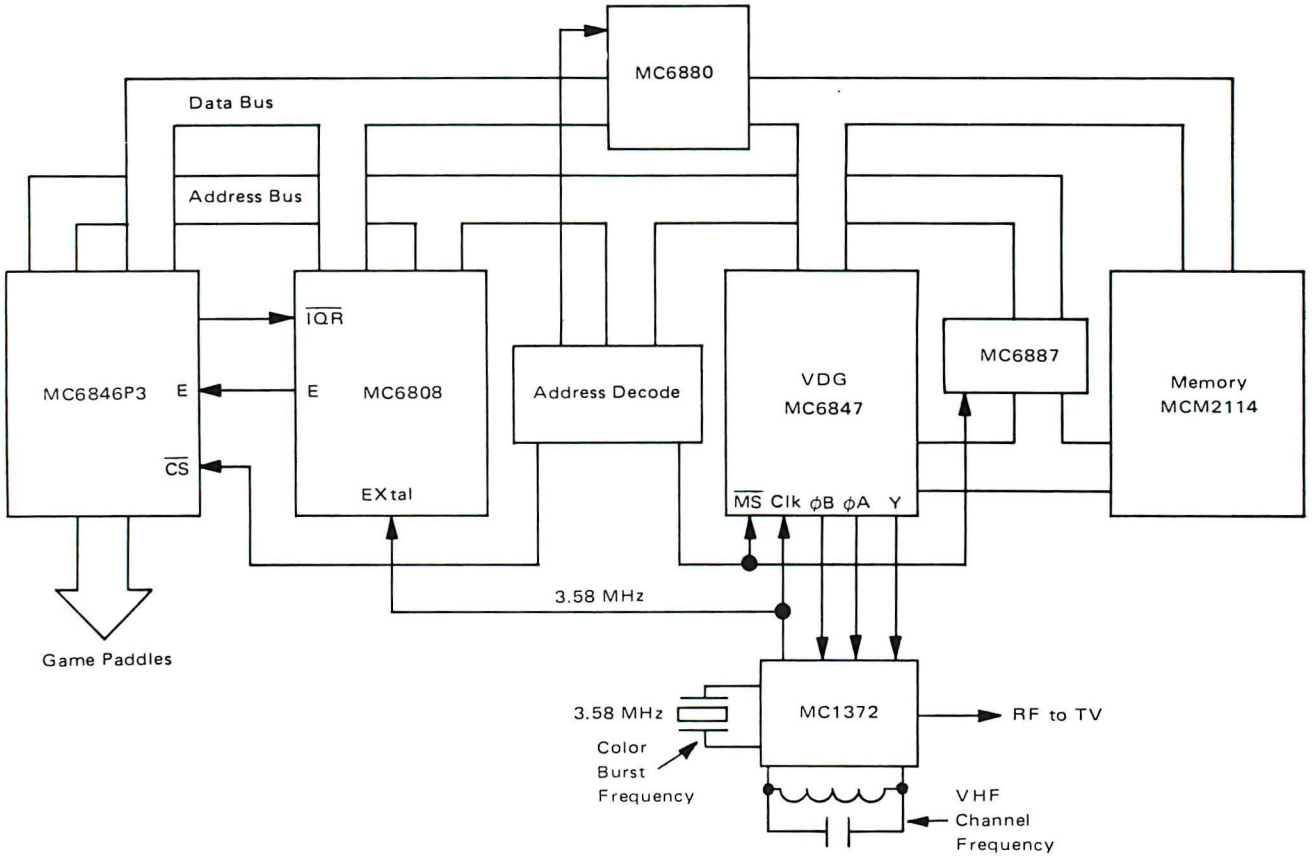


FIGURE 1 – BLOCK DIAGRAM OF USE OF THE VDG IN A TV GAME



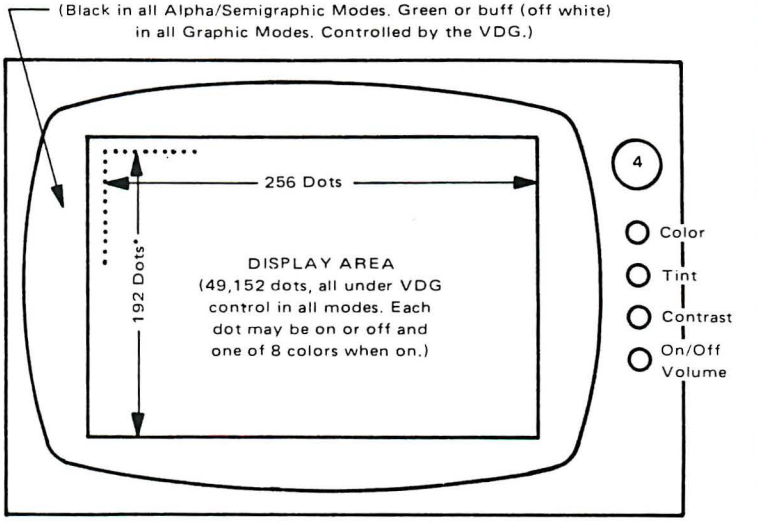
Mnemonic	Pin Numbers	Function
V_{CC}	17	+5V
V_{SS}	1	Ground
CLK	33	Color burst clock 3.579545 MHz (input)
DA0-DA12	22, 23, 24, 25, 26 13, 14, 15, 16, 18, 19, 20, 21	Address lines to display memory, high impedance during memory select ($\overline{MS}$)
DD0-DD5	3, 4, 5, 6, 7, 8	Data from display memory RAM or ROM
DD6, DD7	2, 40	Data from display memory in graphic mode; data also in alpha external mode; color data in alpha semigraphic 4 or 6
$\overline{\phi}$A, ϕB, Y	11, 10, 28	Chrominance and luminance analog (R-Y, B-Y, Y) output to RF modulator (MC1372)
CHB	9	Chroma bias; reference ϕA and ϕB levels
$\overline{RP}$	36	Row preset – Output to provide timing for external character generator.
$\overline{HS}$	38	Horizontal Sync – Output to provide timing for external character generator.
INV	32	Inverts video in all alpha modes
$\overline{INT}$/EXT	31	Switches to external ROM in alpha mode and between SEMIG-4 and SEMIG-6 in semigraphics
$\overline{A}$/S	34	Alpha/Semigraphics; selects between alpha and semigraphics in alpha mode
$\overline{MS}$	12	Memory select forces VDG address buffers to high-impedance state
$\overline{A}$/G	35	Switches between alpha and graphic modes
$\overline{FS}$	37	Field Synchronization goes low at bottom of active display area.
CSS	39	Color set select; selects between two alpha display colors or between two color sets in semigraphics 6 and full graphics
GM0-GM2	30, 29, 27	Graphic mode select; select one of eight graphic modes.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Rating	Value
Supply Voltage (V_{CC})	-0.3 to + 7.0V
Input Voltage any Pin	-0.3 to + 7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-65°C to 150°C
Power Dissipation	TBD

FORMAT OF THE TELEVISION SCREEN



*One on each non-interlaced line.

DC (STATIC) CHARACTERISTICS — (V_{CC} = 5.0 V ±5%, V_{SS} = 0.0 V, T_A = 0°C to 70°C unless otherwise noted)

Characteristic		Symbol	Min	Typ.	Max.	Unit
Input High Voltage Clk Other Inputs		V_{IH}	 V_{SS} + 2.4 V_{SS} + 2.0	 – –	 V_{CC} V_{CC}	Vdc
Input Low Voltage Clk Other Inputs		V_{IL}	 V_{SS} - 0.3 V_{SS} - 0.3	 – –	 V_{SS} + 0.4 V_{SS} + 0.8	Vdc
Input Leakage Current CLK, GM0-GM2, INV, $\overline{INT}$/EXT, $\overline{MS}$, V_{SS}, DD0-DD7, $\overline{A}$/S, $\overline{A}$/G		I_{in}	–	–	2.5	μAdc
Three-State (Off State) Input Current DA0-DA12		I_{LO}	–	–	10	μAdc
Ohtput High Voltage (C_{Load} = 30 pF, I_{Load} = -100 μA)	$\overline{RP}$, $\overline{HS}$, $\overline{FS}$	V_{OH}	2.4	–	–	Vdc
Output High Voltage (C_{Load} = 55 pF, I_{Load} = -100 μA)	DA0-DA12	V_{OH}	2.4	–	–	Vdc
Output Load Voltage (C_{Load} = 30 pF, I_{Load} = 1.6 mA)	$\overline{RP}$, $\overline{HS}$, $\overline{FS}$	V_{OL}	–	–	V_{SS} + 0.4	Vdc
Output Low Voltage (C_{Load} = 55 pF, I_{Load} = 1.6 mA)	DA0-DA12	V_{OL}	–		V_{SS} + 0.4	Vdc
Output High Current (Sourcing) (V_{OH} = 2.4 V)	All Outputs (except φA, φB, Y, & CHB)	I_{OH}	-100	–	–	μAdc
Output Low Current (Sinking) (V_{OL} = 0.4 Vdc)	All Outputs (except φA, φB, Y, & CHB)	I_{OL}	1.6	–	–	mAdc
Input Capacitance (V_{in} = 0, T_A = 25°C, f = 1.0 MHz)	All Inputs	C_{in}	–	–	7.5	pF
Chroma Bias Voltage (C_{Load} = 20 pF, R Load = 200 k ohm, V_{CC} = 4.75 – 5.25 V)		V_R	–	0.3 V_{CC}	–	Vdc

DC (STATIC) CHARACTERISTICS — (V_{CC} = 5.0 V ± 5%, V_{SS} = 0.0 V, T_A = 0°C to 70°C unless otherwise noted)

Characteristic	Symbol	Min	Typ.	Max.	Unit
Chroma φA Voltage Figure 2	$V_{C\phi A}$				Vdc
(C_{Load} = 20 pF, R Load = 200 k ohm)	V_{HI}	–	V_R + 0.1 V_{CC}	–	
	V_0	–	V_R	–	
	V_{LO}	–	V_R – 0.1 V_{CC}	–	
Chroma φB Voltage	$V_{C\phi B}$				Vdc
(C_{Load} = 20 pF, R Load = 200 k ohm)		–	V_R + 0.1 V_{CC}	–	
V_0		–	V_R	–	
V_{burst}		–	V_R – 0.05 V_{CC}	–	
V_{LO}		–	V_R – 0.1 V_{CC}	–	
Luminance Y Voltage Figure 2	V_Y				Vdc
(C_{Load} = 20 pF, R_{Load} = 200 k ohm)	V_S	–	0.2 V_{CC}	–	
	V_{BLANK}	–	0.75 V_S	–	
	V_{BLACK}	–	0.7 V_S	–	
Voltage White Low Figure 2	V_{WL}	–	0.62 V_S	–	Vdc
(Voltage White Medium)	V_{WM}	–	0.5 V_S	–	
(Voltage White High)	V_{WH}	–	0.38 V_S	–	

AC (Dynamic) CHARACTERISTICS — V_{CC} = 5.0 V ± 5%, T_A = 0°C to 70°C

Characteristic	Symbol	Min	Typ.	Max.	Unit
Clk Frequency	f	3.579535	3.579545	3.579555	MHz
Clk Duty Cycle	Clk_{dc}	45%	50%	55%	
Chroma Phase Delay Figure 3C					ns
(measured with respect to "Y" output)					
φA	t_{YA}	–	200	–	
φB	t_{YB}	–	200	–	
Luminance Rise Time Figure 3D	t_{ry}	–	60	–	ns
Luminance Fall Time	t_{fy}	–	50	–	
Chroma Rise and Fall Times Figure 3D					ns
(φA Rise Time)	$t_rC\phi A$	–	60	–	
(φA Fall Time)	$t_fC\phi A$	–	60	–	
(φB Rise Time)	$t_rC\phi B$	–	60	–	
(φB Fall Time)	$t_fC\phi B$	–	60	–	
$\overline{\text{Field Sync.}}$ ($\overline{FS}$) Figure 3A	t_{WFS}	–	2.03	–	ms
(Pulse Width)					
$\overline{\text{Row Present}}$ ($\overline{RP}$) Figure 3B					
(Pulse Width)	t_{WRP}	–	0.98	–	μs
(Delay From $\overline{HS}$)	t_{HSRP}	–	0.98	–	μs
$\overline{\text{Horizontal Sync}}$ ($\overline{HS}$) Figure 3B	t_{WHS}	–	4.9	–	μs

FIGURE 2 – VIDEO AND CHROMINANCE RELATIONSHIPS OUTPUT WAVEFORM

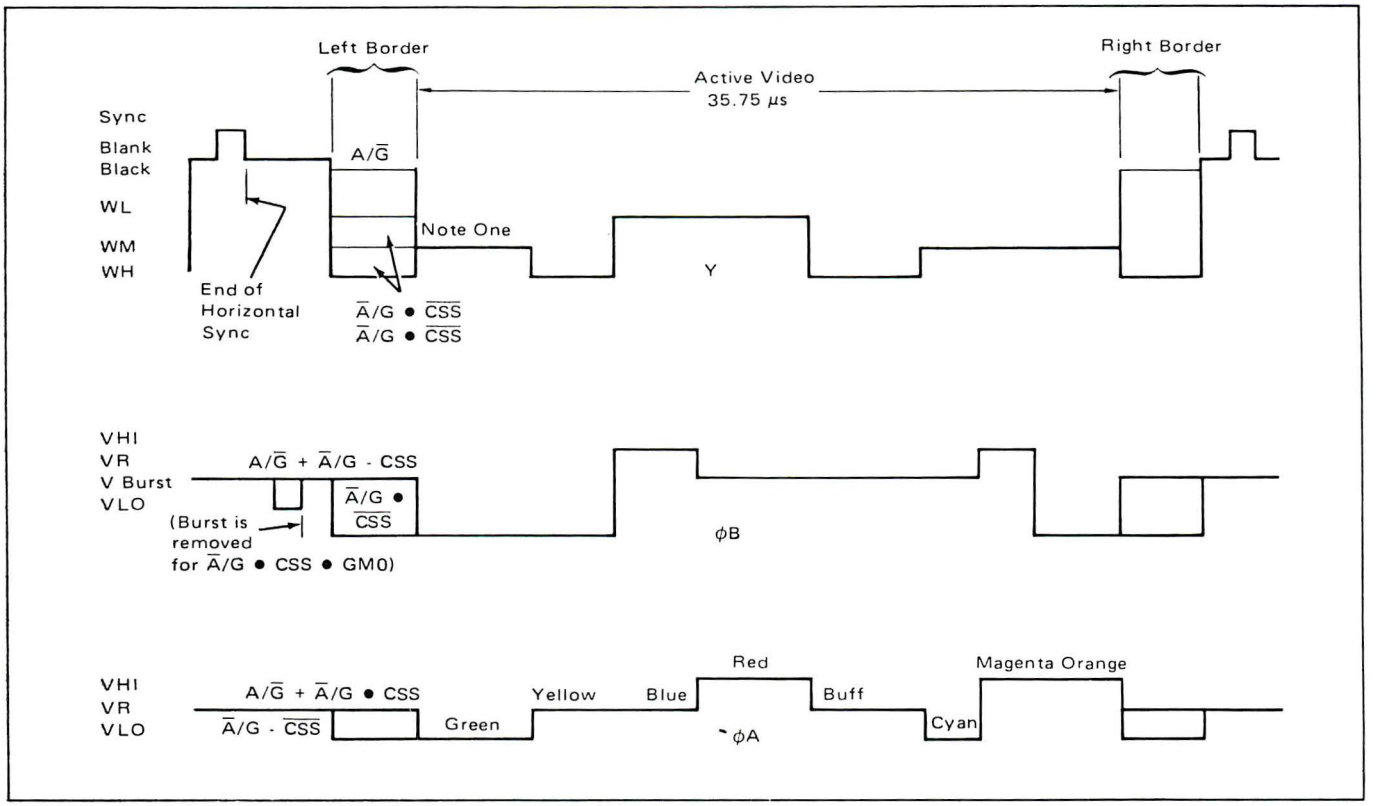
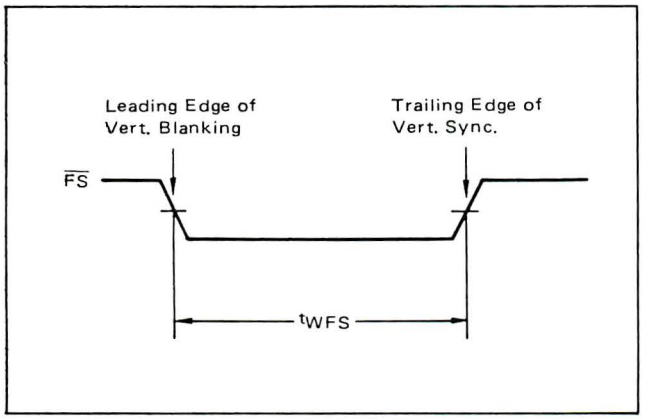
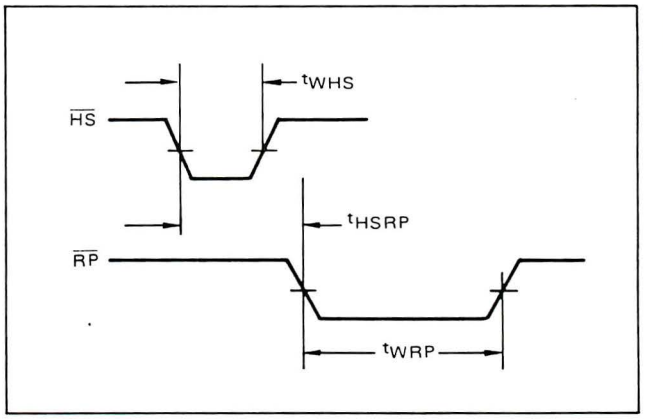


FIGURE 3 – TIMING DIAGRAMS

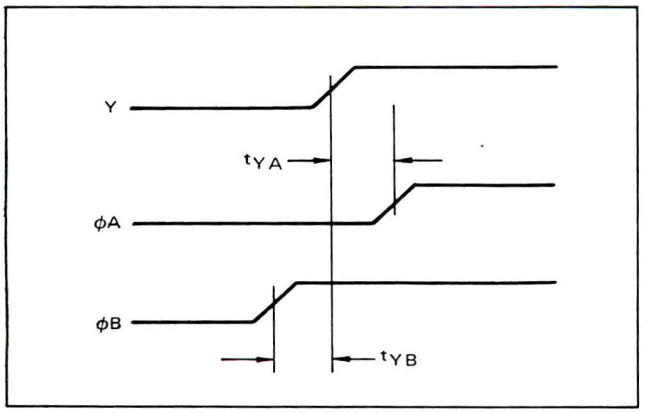
A– Field Sync



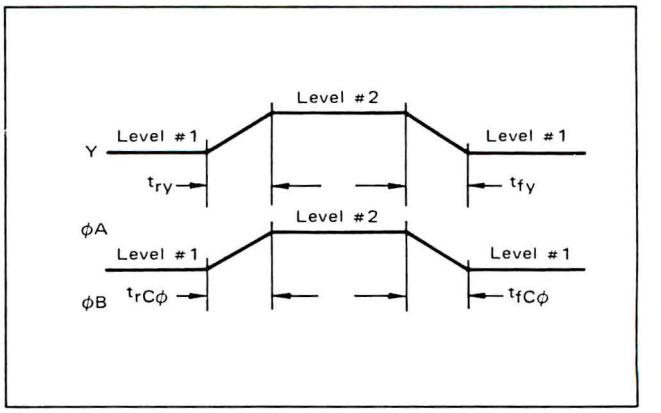
B – Row Preset



C – Chroma Phase Delay



D – Video Rise & Fall Times



VDG SIGNAL DESCRIPTION

Address Output Lines (DA0-DA12) – Thirteen address lines are used by the VDG to scan the display memory. The starting address of the display memory is located at the upper left corner of the display screen. As the television sweeps from the left to right and top to bottom, the VDG increments the RAM display address. These lines are TTL compatible and may be forced into a high impedance state whenever the $\overline{MS}$ pin goes low.

Data Inputs (DD0-DD7) – Eight TTL compatible data lines are used to input data from RAM to be processed by the VDG. The data is interpreted and transformed into luminance Y (Pin 28) and color outputs ϕA and ϕB (Pin 11 and Pin 10).

Power Inputs – V_{CC} requires +5 volts. V_{SS} requires zero volts and is normally ground. The tolerance and current requirements of the VDG are specified in the Electrical Characteristics.

Video Outputs (ϕA, ϕB, Y, CHB) – These four analog outputs are used to transfer luminance and color information to a standard NTSC color television receiver, either via the MC1372 RF modulator or directly into Y, ϕA, ϕB television video inputs.

LUMINANCE (Y) – This six level analog output contains composite sync., blanking and four levels of video luminance.

ϕA – This three level analog output is used in combination with ϕB and Y outputs to specify one of eight colors.

ϕB – This four level analog output is used in combination with ϕA and Y outputs to specify one of eight colors. Additionally, one analog level is used to specify the time of the color burst reference signal.

CHROMA BIAS (CHB) – This pin is an analog output and provides a D.C. reference corresponding to the quiescent value of ϕA and ϕB. CHB is used to guarantee good thermal tracking and minimize the variation between the parts.

Synchronizing Inputs ($\overline{MS}$, CLK)

Three-State Control – ($\overline{MS}$) is a TTL compatible input which, when low, forces the VDG address lines into a high impedance state. This may be done to allow other devices (such as an MPU) to address the display memory (RAM).

Clock (CLK) – The VDG clock input (CLK) requires a 3.579545 MHz (standard) TV crystal frequency square wave. The duty cycle of this clock must be between 45 and 55 percent since it controls the width of alternate dots on the television screen. The MC1372 RF modulator may be used to supply the 3.579545 MHz clock and has provisions for a duty cycle adjustment.

Synchronizing Outputs ($\overline{FS}$, $\overline{HS}$, $\overline{RP}$) – Three TTL compatible outputs provide circuits, exterior to the VDG, with timing references to the following internal VDG states:

FIELD SYNC – ($\overline{FS}$) – The high to low transition of the $\overline{FS}$ output coincides with the end of active display area. During this time interval an MPU may have total access to the display RAM without causing undesired flicker on the screen. The Low to High transition of $\overline{FS}$ coincides with the trailing edge of the vertical synchronization pulse.

HORIZONTAL SYNC – ($\overline{HS}$) – The $\overline{HS}$ pulse is in coincidents with the horizontal synchronization pulse furnished to the television receiver by the VDG. The high to low transition of the $\overline{HS}$ output coincides with the leading edge of the horizontal synchronization pulse.

ROW PRESET – ($\overline{RP}$) – If desired, an external character generator ROM may be used with the VDG. However, an external four bit counter must be added to supply row selection. The counter is clocked by the $\overline{HS}$ signal and cleared by the $\overline{RP}$ signal.

Mode Control Lines (Input) ($\overline{A}$/G, $\overline{A}$/S, $\overline{INT}$/EXT, GM0, GM1, GM2, CSS, INV) – Eight TTL compatible inputs are used to control the operating mode of the VDG. $\overline{A}$/S, $\overline{INT}$/EXT, CSS and INV may be changed on a character by character basis. The CSS pin is used to select between two possible alphanumeric colors; when the VDG is in the alphanumeric mode and between two color sets when the VDG is in the semigraphics 6 and full Graphic mode. Table 1 illustrates the various modes that can be obtained using the mode control lines.

DISPLAY MODES

The VDG is capable of generating 12 distinct display modes (refer to Table 1). The color set selection and invert pins will allow variations on certain modes. The VDG will display two alphanumeric modes with two compatible semigraphic modes or display one of eight full graphic modes. A detailed description of the various modes of operation follows. A summary of major modes can be found in Table 2.

ALPHANUMERIC DISPLAY MODES – All alphanumeric modes occupy an 8 x 12 dot character matrix box and there are 32 x 16 character boxes per TV frame. Each horizontal dot (dot-clock) corresponds to one-half the period duration of the 3.58 MHz clock and each vertical dot is one scan line. One of two colors for the lighted dots may be selected by the color set select pin. An internal ROM will generate 64 ASCII display characters in a standard 5 x 7 box. Six bits of the eight-bit data word are used for the ASCII character generator and the two bits not used can be used to implement inverse video or color switching on a character by character basis. A 512 word display memory is required for this class of display.

The ALPHA SEMIGraphics -4 mode translates bits zero through three into a 4 x 6 dot element in the standard 8 x 12 dot box. Three data bits may be used to select one of eight colors for the entire character box. The extra bit is available to implement mode switching on the fly. A 512 word display memory is required. A density of 64 x 32 elements is available in the display area. The element area is four dot-clocks wide by six lines high.

The ALPHA SEMIGraphic -6 mode maps six 4 x 4 dot elements into the standard 8 x 12 dot alphanumeric box, a screen density of 64 x 48 elements is available. Six bits are used to generate this map and two data bits may be used to select one of four colors in the display box. The element area is four dot-clocks wide by four lines high.

FULL GRAPHIC MODE – There are eight full graphic modes available from the VDG. These modes require 1K to 6K bytes of memory. The eight full-graphic modes include an outside color border in one of two colors depending upon the color set select pin (CSS). The CSS pin selects one of two sets of four colors in the four color graphic modes.

The 64 x 64 Color Graphics Mode – The 64 x 64 color graphics mode generates a display matrix of 64 elements wide by 64 elements high. Each element may be one of four colors. A 1K x 8 display memory is required. Each pictel equals four dot-clocks by three scan lines.

The 128 x 64 Graphics Mode – The 128 x 64 graphics mode generates a matrix 128 elements wide by 64 elements high. Each element may be either ON or OFF. However, the entire display may be one of two colors, selected by using the color set select pin. A 1K x 8 display memory is required. Each pictel equals two dot-clocks by three scan lines.

The 128 x 64 Color Graphics Mode – The 128 x 64 color graphics mode generates a display matrix 128 elements wide by 64 elements high. Each element may be one of four colors. A 2K x 8 display memory is required. Each pictel equals two dot-clocks by three scan lines.

The 128 x 96 Graphics Mode – The 128 x 96 graphics mode generates a display matrix 128 elements wide by 96 elements high. Each element may be either ON or OFF. However, the entire display may be one of two colors selected by using the color select pin. A 2K x 8 display memory is required. Each pictel equals two dot-clocks by two scan lines.

The 128 x 96 Color Graphics Mode – The 128 x 96 color graphics mode generates a display 128 elements wide by 96 elements high. Each element may be one of four colors. A 3K x 8 display memory is required. Each pictel equals two dot-clocks by two scan lines.

The 128 x 192 Graphics Mode – The 128 x 192 graphics mode generates a display matrix 128 elements wide by 192 elements high. Each element may be either ON or OFF, but the ON elements may be one of two colors selected with color set select pin. A 3K x 8 display memory is required. Each pictel equals two dot-clocks by one scan line.

The 128 x 192 Color Graphics Mode – The 128 x 192 color graphics mode generates a display 128 elements wide by 192 elements high. Each element may be one of four colors. A 6K x 8 display memory is required. A detailed description of the VDG modes is given in Table 3. Each pictel equals two dot-clocks by one scan line.

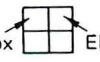
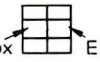
The 256 x 192 Graphics Mode – The 256 x 192 graphics mode generates a display 256 elements wide by 192 elements high. Each element may be either ON or OFF, but the ON element may be one of two colors selected with the color set select pin. A 6K x 8 display memory is required. Each pictel equals one dot-clock by one scan line.

TABLE 1 – TABLE OF MODE CONTROL LINES (INPUTS)

$\overline{A}/G$	$\overline{A}/S$	$\overline{INT}/EXT$	INV	GM2	GM1	GM0	ALPHA/GRAPHIC MODE SELECT
0	0	0	0	X	X	X	Internal Alphanumerics
0	0	0	1	X	X	X	Internal Alphanumerics Inverted
0	0	1	0	X	X	X	External Alphanumerics
0	0	1	1	X	X	X	External Alphanurnerics Inverted
0	1	0	X	X	X	X	Semigraphics - 4
0	1	1	X	X	X	X	Semigraphics - 6
1	X	X	X	0	0	0	64 x 64 Color Graphics
1	X	X	X	0	0	1	128 x 64 Graphics
1	X	X	X	0	1	0	128 x 64 Color Graphics
1	X	X	X	0	1	1	128 x 96 Graphics
1	X	X	X	1	0	0	128 x 96 Color Graphics
1	X	X	X	1	0	1	128 x 192 Graphics
1	X	X	X	1	1	0	128 x 192 Color Graphics
1	X	X	X	1	1	1	256 x 192 Graphics

TABLE 2 – SUMMARY OF MAJOR MODES

MAJOR MODE ONE
TABLE OF ALPHA MINOR MODES

Title	Memory	Colors	Display Elements
Alphanumeric (Internal)	512 x 8	2	
Alphanumeric (External)	512 x 8	2	
Alpha Semig-4	512 x 8	8	Box  Element
Alpha Semig-6	512 x 8	4	Box  Element

MAJOR MODE TWO
TABLE OF MINOR GRAPHICS MODES

Title	Memory	Colors	Comments
64 x 64 Color Graphic	1K x 8	4	Matrix 64 x 64 Elements
128 x 64 Graphics*	1K x 8	2	Matrix 128 elements wide by 64 elements high
128 x 64 Color Graphic	2K x 8	4	
128 x 96 Graphics*	1.5K x 8	2	Matrix 128 elements wide by 96 elements high
128 x 96 Color Graphic	3K x 8	4	
128 x 192 Graphics*	3K x 8	2	Matrix 128 elements wide by 192 elements high
128 x 192 Color Graphic	6K x 8	4	
256 x 192 Graphics*	6K x 8	2	Matrix 256 elements wide by 192 elements high

*Graphics mode turns on or off each element. The color may be one of two.

TABLE 3 – DETAILED DESCRIPTION OF VDG MODES

VDG PINS									COLOR			TV SCREEN		VDG DATA BUS	COMMENTS
$\overline{MS}$	$\overline{A/G}$	$\overline{A/S}$	$\overline{INT}$/EXT	GM2	GM1	GM0	CSS	INV	Character Color	Background	Border	Display Mode	Detail		
1	0	0	0	X	X	X	0	0	Green	Black	Black	32 Characters across 16 Characters down	8 dots, 12 dots, 7, 5	extra, ASCII code	The ALPHANUMERIC INTERNAL mode uses an internal character generator which contains the following five dot by seven dot characters: @ABCDEFGHIJ KLMNOPQRSTUVWXYZ[\] ↑ ← SP !"#$%&'()*+,-./0123456789:;<=>?. The six bit ASCII code leaves two bits free and these may be externally connected to the mode pins ($\overline{A/G}$, $\overline{A/S}$, $\overline{INT}$/EXT, GM2, GM1, GM0, CSS or INV).
								1	Black	Green					
							1	0	Orange	Black	Black				
								1	Black	Orange					
1	0	0	1	X	X	X	0	0	Green	Black	Black	32 Characters across 16 Characters down		one row of custom characters	The ALPHANUMERIC EXTERNAL mode uses an external character generator as well as a row counter. Thus, custom character fonts are graphic symbol sets with up to 256 different eight dot X 12 dot "characters" may be displayed.
								1	Black	Green					
							1	0	Orange	Black	Black				
								1	Black	Orange					
1	0	1	0	X	X	X	X	X	Lx C2 C1 C0 Color 0 X X X Black 1 0 0 0 Green 1 0 0 1 Yellow 1 0 1 0 Blue 1 0 1 1 Red 1 1 0 0 Buff 1 1 0 1 Cyan 1 1 1 0 Magenta 1 1 1 1 Orange		Black	64 Display elements across 32 Display elements down	L_3 L_2 / L_1 L_0 one element	C_2 C_1 C_0 L_3 L_2 L_1 L_0	The SEMIGRAPHICS FOUR mode uses an internal "course graphics" generator in which a rectangle (eight dots by twelve dots) is divided into four equal parts. The luminance of each part is determined by a corresponding bit on the VDG data bus. The color of illuminated parts is determined by three bits.
1	0	1	1	X	X	X	0	X	Lx C1 C0 Color 0 X X Black 1 0 0 Green 1 0 1 Yellow 1 1 0 Blue 1 1 1 Red 0 X X Black 1 0 0 Buff 1 0 1 Cyan 1 1 0 Magenta 1 1 1 Orange		Black	64 Display elements across 48 Display elements down	L_5 L_4 / L_3 L_2 / L_1 L_0	C_1 C_0 L_5 L_4 L_3 L_2 L_1 L_0	The SEMIGRAPHIC SIX mode is similar to the SEMIGRAPHIC FOUR mode with the following differences. The eight dot by twelve dot rectangle is divided into six equal parts. Color is determined by the two remaining bits.
1	1	X	X	0	0	0	0	X	C1 C0 Color 0 0 Green 0 1 Yellow 1 0 Blue 1 1 Red 0 0 Buff 0 1 Cyan 1 0 Magenta 1 1 Orange		Green	64 Display elements across 64 Display elements down	E_3 E_2 E_1 E_0	C_1 C_0 C_1 C_0 C_1 C_0 C_1 C_0	The GRAPHICS ONE C mode uses a maximum of 1024 bytes of display RAM in which one pair of bits specifies one picture element.
							1	X			Buff				
1	1	X	X	0	0	1	0	X	Lx Color 0 Black 1 Green		Green	128 Display elements across 64 Display elements down	L_7 L_6 L_5 L_4 L_3 L_2 L_1 L_0	L_7 L_6 L_5 L_4 L_3 L_2 L_1 L_0	The GRAPHICS ONE R mode uses a maximum of 1024 bytes of display RAM in which one bit specifies one picture element.
							1	X	0 Black 1 Buff		Buff				
1	1	X	X	0	1	0	0	X	Same color as Graphics one C		Green	128 Display elements across 64 Display elements down	E_3 E_2 E_1 E_0	C_1 C_0 C_1 C_0 C_1 C_0 C_1 C_0	The GRAPHICS TWO C mode uses a maximum of 2048 bytes of display RAM in which one pair of bits specifies one picture element.
							1	X			Buff				
1	1	X	X	0	1	1	0	X	Same color as Graphics one R		Green	128 Display elements across 96 Display elements down	L_7 L_6 L_5 L_4 L_3 L_2 L_1 L_0	L_7 L_6 L_5 L_4 L_3 L_2 L_1 L_0	The GRAPHICS TWO R mode uses a maximum of 1536 bytes of display RAM in which one bit specifies one picture element.
							1	X			Buff				
1	1	X	X	1	0	0	0	X	Same color as Graphics one C		Green	128 Display elements across 96 Display elements down	E_3 E_2 E_1 E_0	C_1 C_0 C_1 C_0 C_1 C_0 C_1 C_0	The GRAPHICS THREE C mode uses a maximum of 3072 bytes of display RAM in which one pair of bytes specifies one picture element.
							1	X			Buff				
1	1	X	X	1	0	1	0	X	Same color as Graphics one R		Green	128 Display elements across 192 Display elements down	L_7 L_6 L_5 L_4 L_3 L_2 L_1 L_0	L_7 L_6 L_5 L_4 L_3 L_2 L_1 L_0	The GRAPHICS THREE R mode uses a maximum of 3072 bytes of display RAM in which one bit specifies one picture element.
							1	X			Buff				
1	1	X	X	1	1	0	0	X	Same color as Graphics one C		Green	128 Display elements across 192 Display elements down	E_3 E_2 E_1 E_0	C_1 C_0 C_1 C_0 C_1 C_0 C_1 C_0	The GRAPHICS SIX C mode uses a maximum of 6144 bytes of display RAM in which one pair of bits specifies one picture element.
							1	X			Buff				
1	1	X	X	1	1	1	0	X	Same color as Graphics one R		Green	256 Display elements across 192 Display elements down	L_7 L_6 L_5 L_4 L_3 L_2 L_1 L_0	L_7 L_6 L_5 L_4 L_3 L_2 L_1 L_0	The GRAPHICS SIX R mode uses a maximum of 6144 bytes of display RAM in which one bit specifies one picture element.
							1	X			Buff				

APPENDIX A

Custom MC6847 Ordering Information

A.0 Custom MC6847 Ordering Information

The custom MC6847 specifications may be transmitted to Motorola in any of the following media:

1 PROM(s)
2 Assembler formatted object tape
3 Punched card deck
4 Paper tape of card deck format

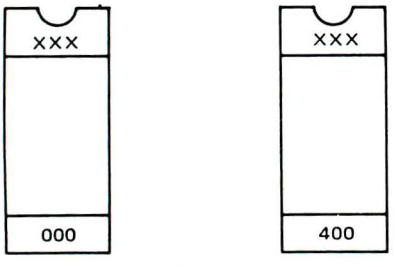
To initiate a ROM pattern for the MC6847 it is necessary to first contact your local field service office, local sales person or your local Motorola representative.

A.1 PROMs

MCM2708 or MCM2716 type PROMs, programmed with the customer program (positive logic sense for address and data), may be submitted for pattern generation. The PROMs must be clearly marked to indicate which PROM corresponds to which address space (000-3FF HEX). See Figure A-1 for recommended marking procedure.

After the PROM(s) are marked they should be placed in conductive IC carriers and securely packed. Do not use styrofoam.

FIGURE A-1



XXX = Customer ID

A.2 Assembler Formatted Object Tape

Cassette tapes produced on a Silent 700 terminal and EXORciser are acceptable.

A.3 Punched Card Deck

The custom MC6847 may be specified for manufacture in the form of standard 80-column punched cards.

The card deck for specifying the Custom MC6847 has the following format:

OPTION CARD
COMMENT CARDS
X CARDS
C CARDS

Option Card — The first card in the deck must be the OPTION CARD. The format is as follows:

Column 1-20: Customer name. Any 20 characters may be used.

Column 25-29: This is a 5-digit number assigned by Motorola. Leave this field blank. It will be punched at Motorola unless otherwise notified.

Column 37-39: Address field base on output listing. The characters HEX or DEC specify the output listing address base as hexadecimal or decimal, respectively. If omitted, DEC is assumed.

Column 41-43: Data field base on output listing. The characters HEX or DEC specify the output listing ROM data base as hexadecimal or decimal, respectively. If omitted, DEC is assumed.

Comment Cards — Comment Cards must have an asterisk (*) in column 1. The remaining 79 columns may contain any letter, number, or character.

X Cards — Five X cards are possible. All X cards have an X in column 1 and one or three or more words each separated by one blank space.

The possibilities are:

1) X SEQUENCE
2) X BASE DEC DEC
3) X BASE DEC HEX
4) X BASE HEX DEC
5) X BASE HEX HEX

Card 1 specifies that there are sequence numbers on each data card that follows. The sequence numbers must be in columns 77-79 of the data cards (C Cards) and must be in decimal, right justified. The numbers must start with 1 (one) and must be in order. The X SEQUENCE Card may appear anywhere within the deck after the Option Card. If it appears within the data card section, data cards encountered before the X SEQUENCE Card will not be checked for sequence numbers. All following cards will be checked. If no X SEQUENCE Card is used, no sequence numbers will be checked.

It is initially assumed that the address and byte count as well as the data specified on the C Cards will be in decimal. An X BASE Card can be used to override this

specification. The second word on the card (that following BASE) specifies the base (either DEC or HEX) of the address and byte count on all following C cards. The last word specifies the base of the data fields on the C Cards. An X BASE Card may appear anywhere within the deck following the OPTION Card. It may be overridden by another X BASE Card. All data cards (C Cards) following an X BASE Card will be interpreted as per that X BASE Card unless another X BASE Card is encountered. If no X BASE Cards are used, it is assumed that all fields on the C Cards are in decimal.

NOTE: Once an X SEQUENCE Card is encountered, all successive cards will be checked for the proper sequence number and unlike X BASE Cards this option cannot thereafter be altered by another X SEQUENCE Card.

C Cards — These cards contain the actual ROM data. All fields are right-justified.

Column 1: C (the letter C)
Column 2-9: ADD
Column 10-12: BYTE
Column 14-16: DATA 1
Column 17-19: DATA 2
•
•
•
Column 76-78: DATA 21
Column 77-79: DATA 22 or SEQUENCE NUMBER

ADD is the address of the first byte of data (DATA 1) contained on that card. Byte is the number of bytes of data to be read from that card. BYTE must be greater than zero and less than 23 (1-22) if no sequence numbers are used, and less than 22 (1-21) if sequence numbers are used. If, for example, there are ten data fields punched on the card, buy BYTE = 2, only the first two will be read. Also, if there are two punched data fields, for example, and BYTE = 6, six ROM locations will be filled from that card. The four unspecified fields will be decoded as zero. ADD and BYTE are always in the same base (HEX or DECIMAL). DATA 1 through DATA N is the data to be placed in the ROM at addresses ADD through ADD + (N-1), respectively.

Any ROM address not filled as a result of reading data from a C Card will be filled with zero. If a particular location has already been specified by a C Card, but a successive C Card also has the data which is to be placed in that location, the second C Card will override the first.

A.4 Paper Tape of Card Deck Format

Punched Paper tape (ASCII) in the same format as cards can also be accepted. However, your order will be processed faster if the data is in card format. After the tape leader there should be a CR LF. Data records should be a full 80 columns, each terminated by a CR LF. Following the last Data record, there should be one more record with the first three characters being EOF, followed by 77 blanks and a CR LF.

CR = Carriage Return
LF = Line Feed

FIGURE A-2

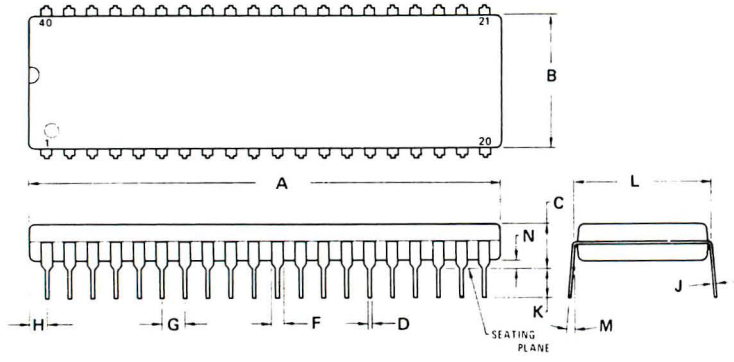
Customer Name _____
Address _____
City _____ State _____ Zip _____
Phone (_____) _____ Extension _____
Contact Ms/Mr _____
Customer Part Number _____

Pattern Media
2708 PROM
2716 PROM
Paper Object Tape
Silent 700 Cassette
Card Deck
Tape of Card Deck
(Note 2) _____

Notes: (2) Other media require prior factory approval

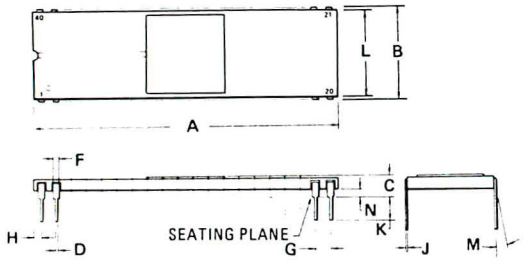
Signature _____
Title _____

P SUFFIX
PLASTIC PACKAGE
CASE 711-02



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	51.82	52.32	2.040	2.060
B	13.72	14.22	0.540	0.560
C	4.57	5.08	0.180	0.200
D	0.36	0.51	0.014	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.30	0.008	0.012
K	3.05	3.56	0.120	0.140
L	15.24 BSC		0.600 BSC	
M	0°	10°	0°	10°
N	0.51	1.02	0.020	0.040

CASE 711-02



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	50.29	51.31	1.980	2.020
B	14.86	15.62	0.585	0.615
C	2.54	4.19	0.100	0.165
D	0.38	0.53	0.015	0.021
F	0.76	1.40	0.030	0.055
G	2.54 BSC		0.100 BSC	
H	0.76	1.78	0.030	0.070
J	0.20	0.33	0.008	0.013
K	2.54	4.19	0.100	0.165
L	14.60	15.37	0.575	0.605
M	0°	10°	0°	10°
N	0.51	1.52	0.020	0.060

CASE 715-02

NOTE:
1. LEADS, TRUE POSITIONED WITHIN 0.25 mm (0.010) DIA (AT SEATING PLANE), AT MAX. MAT'L CONDITION.

L SUFFIX
CERAMIC PACKAGE
CASE 715-02

MOTOROLA *Semiconductor Products Inc.*
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Appendix II

Motorola Color TV Video Modulator Circuits

MOTOROLA
SEMICONDUCTORS
P.O. BOX 20912 • PHOENIX, ARIZONA 85036

MC1372

COLOR TV VIDEO MODULATOR

. . . an integrated circuit used to generate an RF TV signal from baseband color-difference and luminance signals.

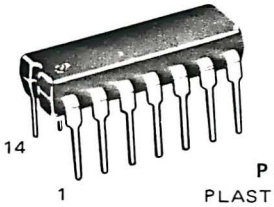
The MC1372 contains a chroma subcarrier oscillator, lead and lag network, a quasi-quadrature suppressed carrier DSB chroma modulator, an RF oscillator and modulator, and a TTL compatible clock driver with adjustable duty cycle.

The MC1372 is a companion part to the MC6847 Video Display Generator, providing and accepting the correct dc interconnection levels. This device may also be used as a general-purpose modulator with a variety of video signal generating devices such as video games, test equipment, video tape recorders, etc.

- Single 5.0 Vdc Supply Operation for NMOS and TTL Compatibility
- Minimal External Components
- Compatible with MC6847 Video Display Generator
- Sound Carrier Addition Capability
- Modulates Channel 3 or 4 Carrier with Encoded Video Signal
- Low Power Dissipation
- Linear Chroma Modulators for High Versatility
- Composite Video Signal Generation Capability
- Ground-Referenced Video Prevents Overmodulation

COLOR TV VIDEO MODULATOR CIRCUIT

SILICON MONOLITHIC INTEGRATED CIRCUIT



P SUFFIX
PLASTIC PACKAGE
CASE 646

Pin Connections

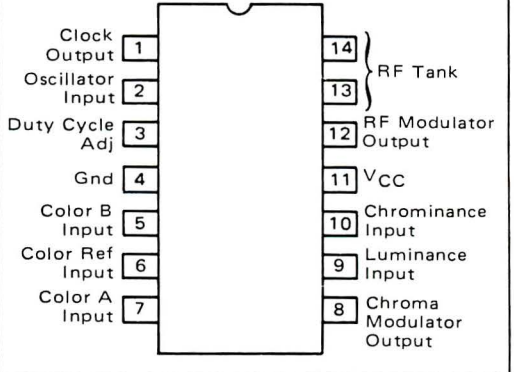
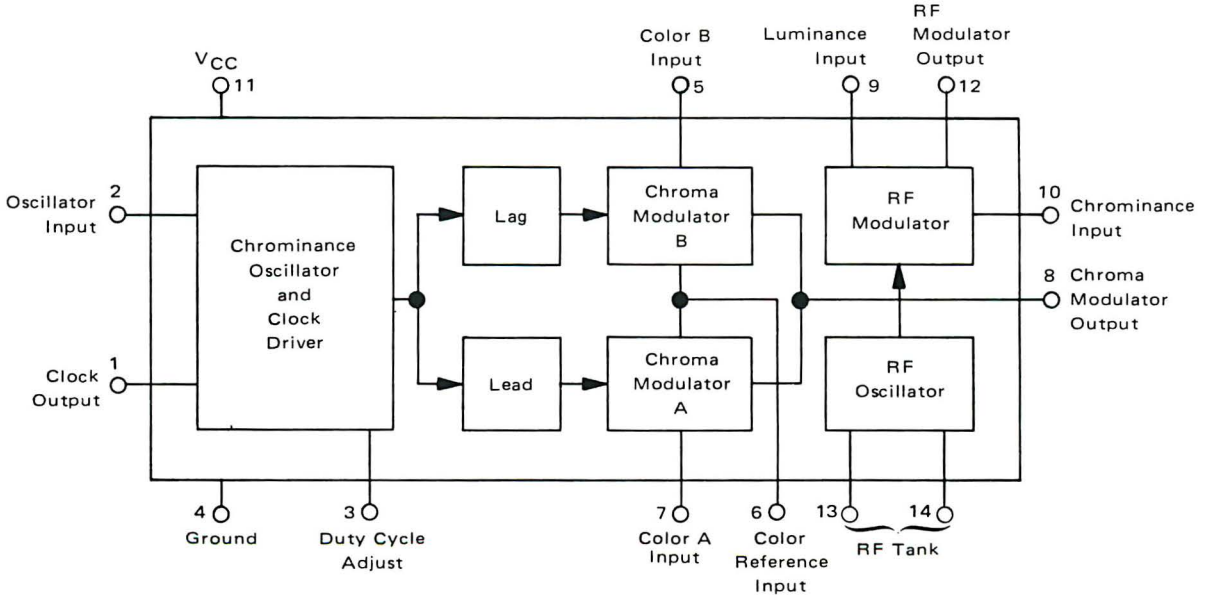


FIGURE 1 – BLOCK DIAGRAM



MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Value	Unit
Supply Voltage	8.0	Vdc
Operating Ambient Temperature Range	0 to +70	°C
Storage Temperature Range	−65 to +150	°C
Junction Temperature	150	°C
Power Dissipation, Package Derate above 25°C	1.25 13	Watts mW/°C

RECOMMENDED OPERATING CONDITIONS

Supply Voltage	5.0	Vdc
Luma Input Voltage — Sync Tip Peak White	1.0 0.35	Vdc
Color Reference Voltage	1.5	Vdc
Color A, B Input Voltage Range	1.0 to 2.0	Vdc

ELECTRICAL CHARACTERISTICS (V_{CC} = +5 Vdc, T_A = 25°C, Test Circuit 1 unless otherwise noted)

Characteristic	Min	Typ	Max	Unit
Operating Supply Voltage	4.75	5.0	5.25	Volts
Supply Current	–	25	–	mA
CHROMA OSCILLATOR/CLOCK DRIVER (Measured at Pin 1 unless otherwise noted)				
Output Voltage (V_{OL}) (V_{OH})	– 2.4	– –	0.4 –	Vdc
Rise Time (V1 = 0.4 to 2.4 Vdc)	–	–	50	ns
Fall Time (V1 = 2.4 to 0.4 Vdc)	–	–	50	ns
Duty Cycle Adjustment Range (V3 = 5.0 Vdc) (Measured at V1 = 1.4 V)	70	–	30	%
Inherent Duty Cycle (No connection to Pin 3)	–	50	–	%
CHROMA MODULATOR (V5 = V6 = V7 = 1.5 Vdc unless otherwise noted)				
Input Common Mode Voltage Range (Pins 5, 6, 7)	0.8	–	2.3	Vdc
Oscillator Feedthrough (Measured at Pin 8)	–	15	31	mV(p-p)
Modulation Angle [θ8(V7 = 2.0 Vdc) − θ8(V5 = 2.0 Vdc)]	85	100	115	degrees
Conversion Gain [V8/(V7 − V6); V8/(V5 − V6)]	–	0.6	–	V(p-p)/Vdc
Input Current (Pins 5, 6, 7)	–	–	−20	μA
Input Resistance (Pins 5, 6, 7)	100	–	–	kΩ
Input Capacitance (Pins 5, 6, 7)	–	–	5.0	pF
Chroma Modulator Linearity (V5 = 1.0 to 2.0 V; V7 = 1.0 to 2.0 V)	–	4.0	–	%
RF MODULATOR				
Luma Input Dynamic Range (Pin 9, Test Circuit 2)	0	–	1.5	Volts
RF Output Voltage (f = 67.25 MHz, V9 = 1.0 V)	–	15	–	mVrms
Luma Conversion Gain (ΔV12/ΔV9; V9 = 0.1 to 1.0 Vdc) Test Circuit 2	–	0.8	–	V/V
Chroma Conversion Gain (ΔV12/ΔV10; V10 = 1.5 Vp-p; V9 = 1.0 Vdc) Test Circuit 2	–	0.95	–	V/V
Chroma Linearity (Pin 12, V10 = 1.5 Vp-p) Test Circuit 2	–	1.0	–	%
Luma Linearity (Pin 12, V9 = 0 to 1.5 Vdc) Test Circuit 2	–	2.0	–	%
Input Current (Pin 9)	–	–	−20	μA
Input Resistance (Pin 10)	–	800	–	Ω
Input Resistance (Pin 9)	100	–	–	kΩ
Input Capacitance (Pins 9, 10)	–	–	5.0	pF
Residual 920 kHz (Measured at Pin 12) See Note 1	–	50	–	dB
Output Current (Pin 12, V9 = 0 V) Test Circuit 2	–	1.0	–	mA
TEMPERATURE CHARACTERISTICS (V_{CC} = 5 Vdc, T_A = 0 to 70°C, IC only)				
Chroma Oscillator Deviation (f_o = 3.579545 MHz)	–	±50	–	Hz
RF Oscillator Deviation (f_o = 67.25 MHz)	–	±250	–	kHz
Clock Drive Duty Cycle Stability	±5.0	–	–	%

NOTE 1. V9 = 1.0 Vdc, V_C = 300 mV(p-p) @ 3.58 MHz,
V_S = 250 mV(p-p) @ 4.5 MHz, Source Impedance = 75 Ω.

FIGURE 2 – TEST CIRCUIT 1

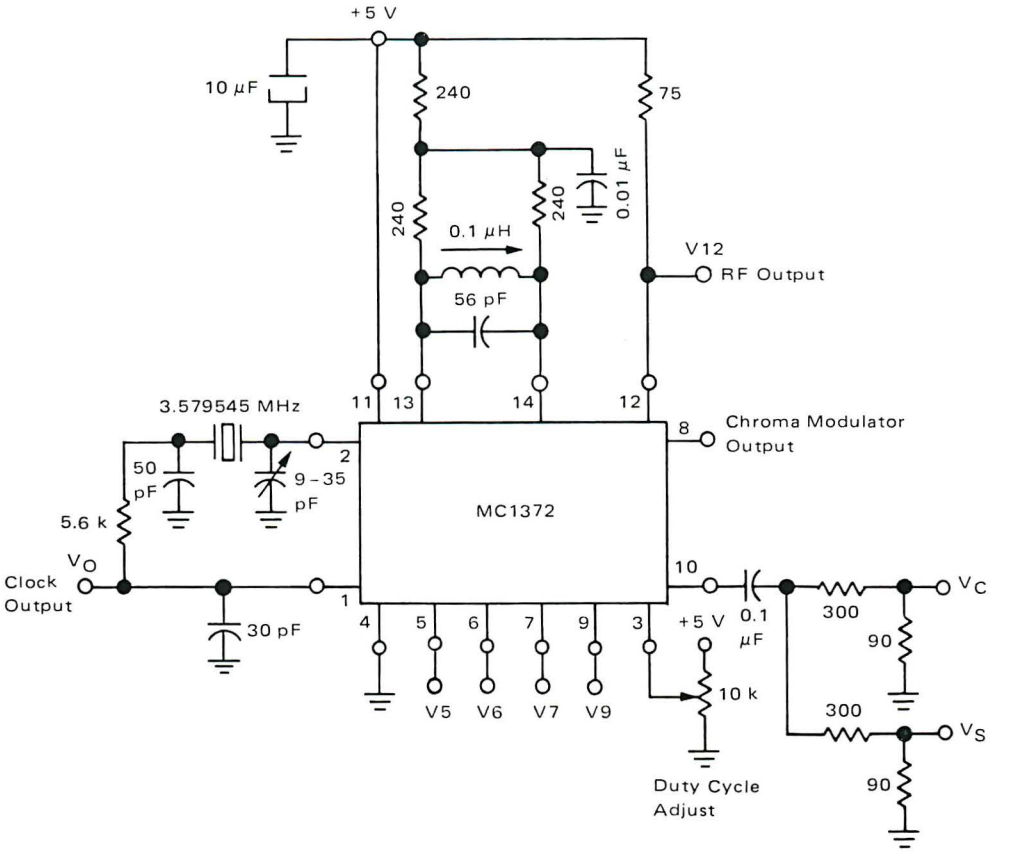


FIGURE 3 – TEST CIRCUIT 2

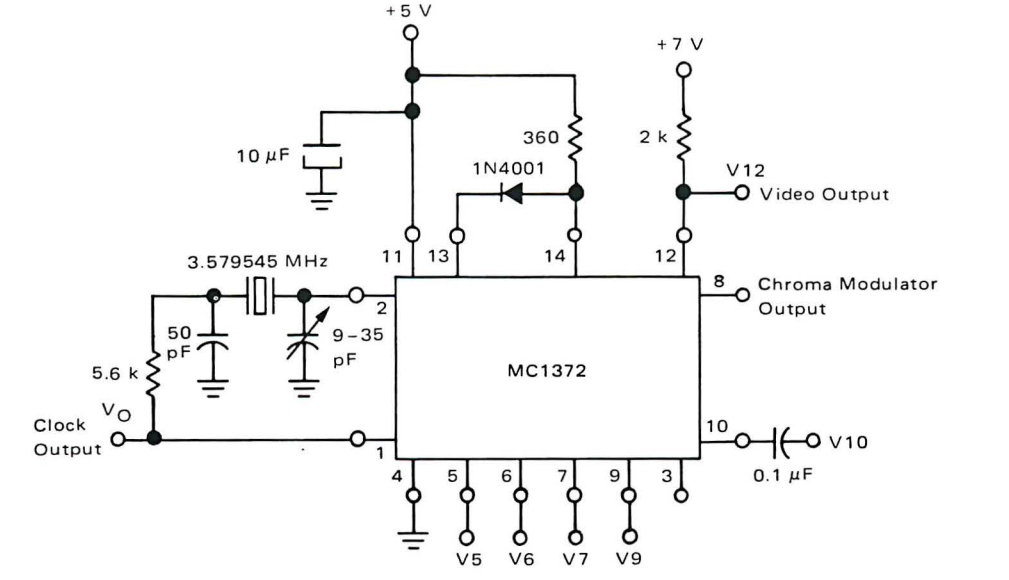
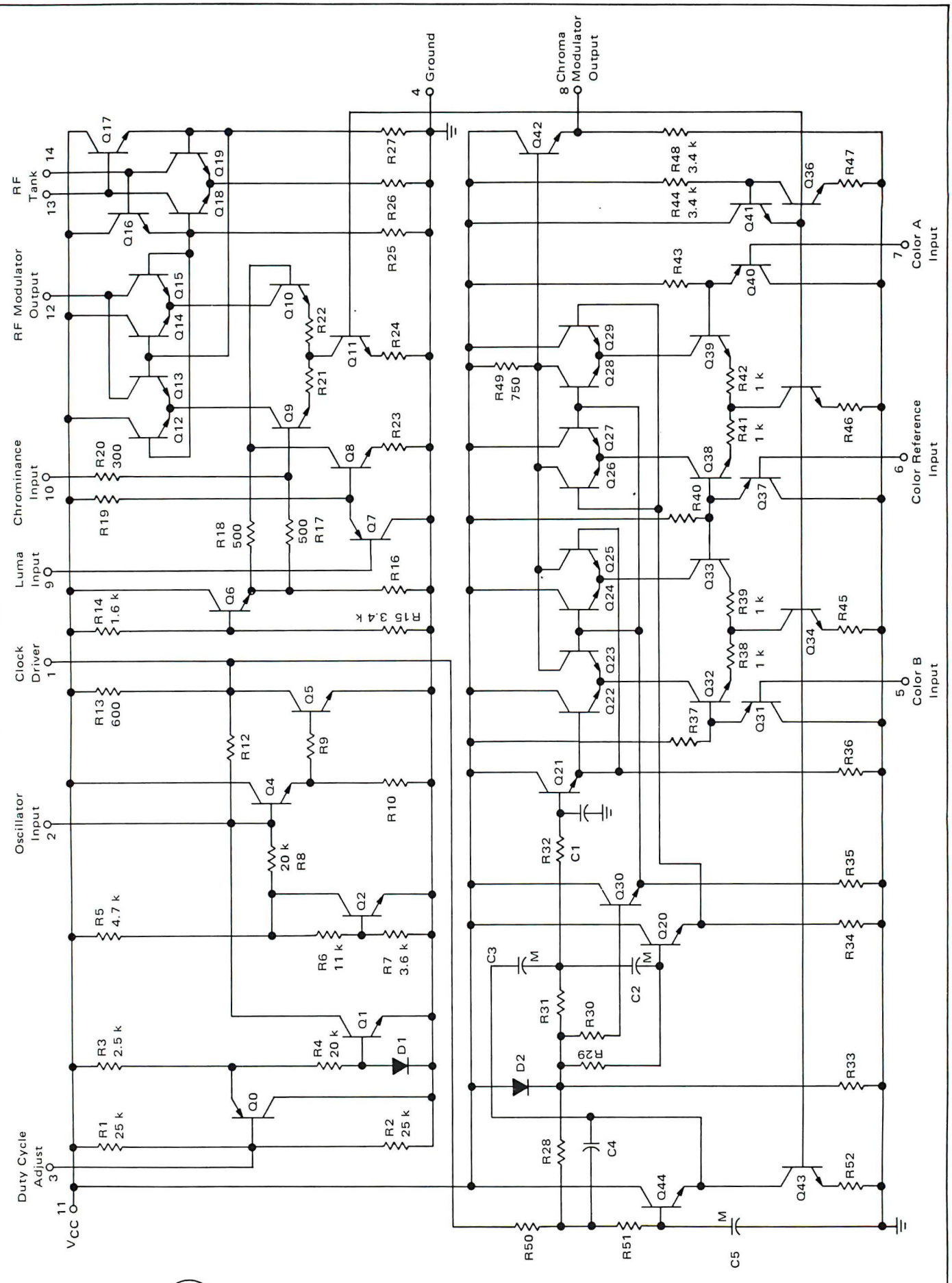


FIGURE 4 – SCHEMATIC DIAGRAM



OPERATIONAL DESCRIPTION

Pin 1 – Clock Output

Provides a rectangular pulse output waveform with frequency equal to the chrominance subcarrier oscillator. This output is capable of driving one LS-TTL load.

Pin 2 – Oscillator Input

Color subcarrier oscillator feedback input. Signal from the clock output is externally phase shifted and ac coupled to this pin.

Pin 3 – Duty Cycle Adjust

A dc voltage applied to this pin adjusts the duty cycle of the clock output signal. If the pin is left unconnected, the duty cycle is approximately 50%.

Pin 4 – Ground

Pin 5 – Color B Input

Dc coupled input to Chroma Modulator B, whose phase leads modulator A by approximately 100^{o}. The modulator output amplitude and polarity correspond to the voltage difference between this pin and the Color Reference Voltage at Pin 6.

Pin 6 – Color Reference Input

The dc voltage applied to this pin establishes the reference voltage to which Color A and Color B inputs are compared.

Pin 7 – Color A Input

Dc coupled input to Chroma Modulator A, whose phase lags modulator B by approximately 100^{o}. The modulator output amplitude and polarity correspond to the voltage difference between this pin and the Color Reference Voltage at Pin 6.

Pin 8 – Chroma Modulator Output

Low impedance (emitter follower) output which provides the vectorial sum of chroma modulators A and B.

Pin 9 – Luminance Input

Input to RF modulator. This pin accepts a dc coupled luminance and sync signal. The amplitude of the RF signal output increases with positive voltage applied to the pin, and ground potential results in zero output (i.e., 100% modulation). A signal with positive-going sync should be used.

Pin 10 – Chrominance Input

Input to the RF modulator. This pin accepts ac coupled chrominance provided by the Chroma Modulator Output (pin 8). The signal is reduced by an internal resistor divider before being applied to the RF modulator. The resistor divider consists of a 300 ohm series resistor and a 500 ohm shunt resistor. Additional gain reduction may be obtained by the addition of external series resistance to pin 10.

Pin 11 – V_{CC}

Positive supply voltage

Pin 12 – RF Modulator Output

Common collector of output modulator stage. Output impedance and stage gain may be selected by choice of resistor connected between this pin and dc supply.

Pins 13 and 14 – RF Tank

A tuned circuit connected between these pins determines the RF oscillator frequency. The tuned circuit must provide a low dc resistance shunt. Applying a dc offset voltage between these pins results in baseband composite video at the RF Modulator Output.

MC1372 CIRCUIT DESCRIPTION

The chrominance oscillator and clock driver consist of emitter follower Q4 and inverting amplifier Q5. Signal presented at clock driver output pin 1 is coupled to oscillator input pin 2 through an external RC and crystal network, which provides 180^{o} phase shift at the resonant frequency. The duty cycle of the output waveform is determined by the dc component at pin 1 internally coupled through R12 to the base of Q4. As pin 1 dc voltage increases, a smaller portion of the sinusoidal feedback signal at pin 2 exceeds the Q4 base voltage of two times V_{BE} required for conduction. As the dc level is reduced, device Q4 and thus Q5 is turned on for a longer percentage of the cycle. Transistors Q0, Q1, Q2 and diode D1 provide the biasing network which determines the dc operating level of the oscillator. The transistor Q2 and resistors R5, R6, and R7 form a voltage reference of four times V_{BE} at the collector of Q2. The dc voltage at pin 1 is determined by the values of R4, R8, and R12 and the applied duty cycle adjust voltage at pin 3. Since these resistors are nominally equal, the voltage at pin 1 will always approximate the dc voltage at pin 3.

The oscillator signal at pin 1 is internally coupled to active filter Q44. This filter reduces the frequency content above 4 MHz. The output of the filter at the emitter of Q44 is ac coupled through C3 to the input of the lead/lag network. R32 and C1 provide approximately 50^{o} of phase lag, while C2 and R29 provide approximately 50^{o} of phase lead. These two quasi-quadrature waveforms are used to switch chroma modulators B and A, respectively. The transistors Q22 through Q25 and Q32–Q33 form a doubly balanced modulator. The input signal applied at pin 5 is compared to the color dc reference voltage applied at pin 6 in differential amplifier Q32–Q33. The source current provided by transistor Q34 is partitioned in transistors Q32 and Q33 according to the differential input signal. The bases of transistors Q23 and Q24 are connected to the dc reference voltage at the emitter of Q30. The bases of transistors Q22 and Q25 are connected

to the phase delayed oscillator signal at the emitter of buffer transistor Q21. The differential signal currents provided by Q32 and Q33 are switched in transistors Q22 through Q25 and the resultant signal voltage is developed across R49. This signal has the phase and frequency of the oscillator signal at the emitter of Q21. The amplitude is proportional to the differential input signal applied between pins 5 and 6. Transistors Q26 through Q29 and Q38–Q39 form chroma modulator B. This modulator develops a signal voltage which is proportional to the differential voltage applied between pins 7 and 6. The phase and frequency of the output is equal to the phase advanced chroma oscillator at the emitter of buffer transistor Q20. Both chroma modulators A and B share the same output resistor, R49, so the output signal presented at the emitter of Q42 (pin 8) is the algebraic sum of modulators A and B.

The RF oscillator consists of differential amplifier Q18 and Q19 cross-coupled through emitter followers Q16 and Q17. The oscillator will operate at the parallel resonant frequency of the network connected between pins 13 and 14. The oscillator output is used to switch the doubly balanced RF modulator, Q9 through Q15. Transistors Q7 and Q9 provide level shifting and a high input impedance to the luminance input pin 9. The bases of transistors Q9 and Q10 are both biased through resistors R17 and R18, respectively, to the same dc reference voltage at Q6 emitter. The base voltage at Q10 may only be offset in a negative direction by luminance signal current source Q8. This design insures that overmodulation due to the luminance signal will never occur. The chrominance signal developed at pin 8 is externally ac coupled to pin 10 where it is reduced by resistor dividers R20 and R17, and added to the luminance signal in Q9. The resultant differential composite video currents are switched at the appropriate RF frequency in Q12 through Q15. The output signal current is presented at pin 12.

Transistors Q36, Q41 and resistors R44, R47 provide a highly stable voltage reference for biasing current sources Q43, Q34, Q35, and Q11.

MC1372 APPLICATION INFORMATION

Chrominance Oscillator

The oscillator is used as a clock signal for driving associated external circuitry, in addition to providing a switching signal for the chroma modulators. The IC uses an external crystal in a Colpitts configuration, as shown in Figure 5. Resistor R1 provides current limiting to reduce the signal swing. Capacitor C2 is adjusted for the exact frequency desired (3.579545 MHz).

In some applications, the duty cycle of the clock signal at pin 1 must be modified to overcome gate delays in associated equipment. The duty cycle may be adjusted by varying the dc voltage applied to pin 3. This adjustment may be made with the use of a potentiometer (10 kΩ) between supply and ground. With no connection to pin 3, the duty cycle is approximately 50%.

Chroma Modulator

The chrominance oscillator is internally phase shifted and applied to chroma modulators A and B. No external lead/lag networks are necessary. The phase relationship between the modulators is approximately 100°, which was chosen to provide the best rendition of colors using equal amplitude color-difference signals. The voltage applied to pin 5, 6, or 7 must always be within the Input Common Mode Voltage Range. Since the amplitude of chrominance output is proportional to the voltage difference between pins 5 and 6 or 7 and 6, it is desirable to select the Color Reference Voltage applied to pin 6 to be midway between $V5_{max}$ and $V5_{min}$ (which should be $V7_{max}$ and $V7_{min}$). The Chroma B Modulator will be defined as a (B-Y) modulator if a burst flag signal is applied to the Color B Input (pin 5) at the appropriate time. This voltage should be negative with respect to the Color Reference Voltage, and typically has an amplitude equal to $1/2[V6-V5_{min}]$. Since the phase of burst is always defined as –(B-Y), the Chroma A Modulator approximates an (R-Y) modulator; however, the phase is offset by 10° from the nominal 90°, to provide the 100° phase shift as discussed previously.

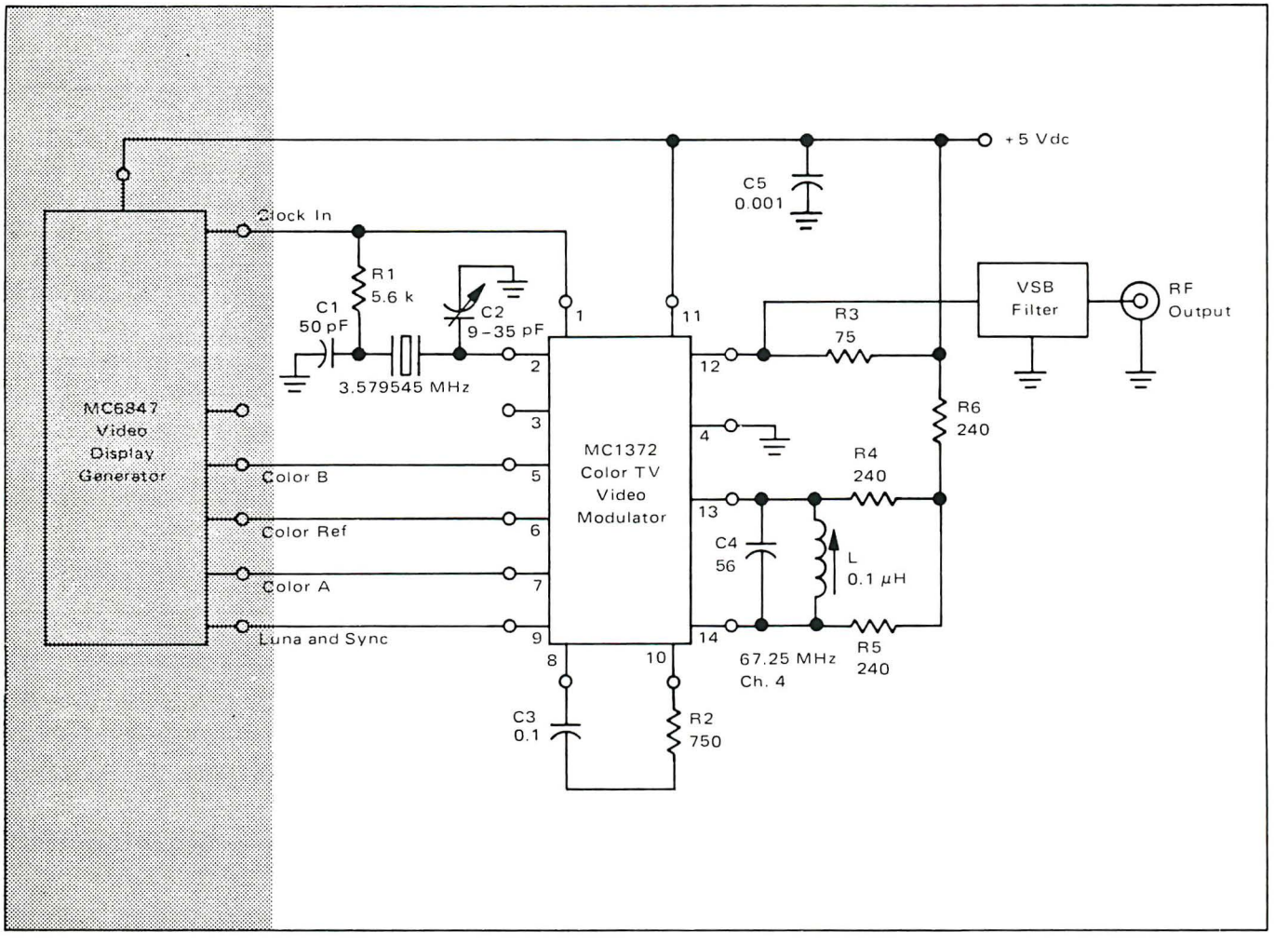
RF Modulator and Oscillator

The coil and capacitor connected between pins 13 and 14 should be selected to have a parallel resonance at the carrier frequency of the desired TV channel. The values of 56 pF and 0.1 μH shown in Figure 5 were chosen for a Channel 4 carrier frequency of 67.25 MHz. For Channel 3 operation, the resonant frequency should be 61.25 MHz (C = 75 pF, L = 0.1 μH). Resistors R4 and R5 are chosen to provide an adequate amplitude of switching voltage, whereas R6 is used to lower the maximum dc level of switching voltage below V_{CC}, thus preventing saturation within the IC.

Composite Luminance and Sync should be dc coupled to Luminance Input, pin 9. This signal must be within the Luma Input Dynamic Range to insure linearity. Since an increase in dc voltage applied to pin 9 results in an increase in RF output, the input signal should have positive-going sync to generate an NTSC compatible signal. As long as the input signal is positive, overmodulation is prevented by the integrated circuit.

Chrominance information should be ac coupled to Chrominance Input, pin 10. This pin is internally connected to a resistor divider consisting of a series 300 ohms and a shunt 500 ohms resistor. The input impedance is thus 800 ohms, and a coupling capacitor should be appropriately chosen.

FIGURE 5 – TYPICAL APPLICATION CIRCUIT



The Luminance to Chrominance ratio (L:C) may be modified with the addition of an external resistor in series with pin 10 (as shown in Figure 5). The unmodified L:C (A_o) is determined by the ratio of the respective Conversion Gain for equal amplitude signals (typically, 0.883 = −1.6 dB). The modified L:C will be governed by the equation $A_o(1 + R_{ext}/800)$ for equal amplitude input signals.

The internal chrominance modulators are not internally connected to the RF modulator; therefore, the user has the option of connecting an externally generated chrominance signal to the RF modulator. In addition, the RF modulator is wideband, and a 4.5 MHz FM audio signal may be added to the chrominance input at pin 10. This may be accomplished by selecting an appropriate series input resistor to provide the correct Luminance:Sound ratio.

The modulated RF signal is presented as a current at RF Modulator Output, pin 12. Since this pin represents a current source, any load impedance may be selected for matching purposes and gain selection, as long as the voltage at pin 12 is high enough to prevent the output devices from reaching saturation (approximately 4.5 V with components in Figure 5). The peak current out of pin 12 is typically 2 mA. Hence, a load resistance of up to 250 ohms may be safely used with a 5 V supply.

Composite Video Signal Generation

The RF modualtor may be easily used as a composite video generator by replacing the RF oscillator tank circuit with a diode as shown in Figure 3. This results in the output modulator being biased so the summation of luminance and chrominance appears unswitched at pin 12. The polarity of the output waveform is controlled by the direction of the diode. *Inverted video:* Anode to pin 14, cathode to pin 13. *Non-inverted video:* Anode to pin 13, cathode to pin 14. Note that the supply resistor must always be connected to the anode of the diode.

The amplitude of signal may be increased by increasing the load resistor on pin 12 and returning it to a higher supply voltage. Any voltage up to the Absolute Maximum Rating may be used.

Applications with MC6847 Video Display Generator

The MC1372 may be easily interfaced to the MC6847 as shown in Figure 5. The dc levels generated and required by the VDG are compatible with the MC1372, so that pins 1, 5, 6, 7, and 9 may be directly coupled to the appropriate MC6847 pins. Both integrated circuits as well as any associated NMOS MPU may be driven from a common 5 Vdc supply.

Recommended Chroma-Luma Signals

A chroma modulation angle of 100° was chosen to facilitate a desirable selection of colors with a minimum number of input signal levels. The following table demonstrates applicable signal levels for a variety of colors.

RECOMMENDED CHROMA-LUMA SIGNALS

	Pin #9 Luminance Input (Vdc)	Pin #7 Color A (Vdc)	Pin #6 Color Ref. (Vdc)	Pin #5 Color B (Vdc)
Sync	1.0	1.5	1.5	1.5
Blanking	0.75	1.5	1.5	1.5
Burst	0.75	1.5	1.5	1.25
Black	0.70	1.5	1.5	1.5
Green	0.50	1.0	1.5	1.0
Yellow	0.38	1.5	1.5	1.0
Blue	0.62	1.5	1.5	2.0
Red	0.62	2.0	1.5	1.5
Cyan	0.50	1.0	1.5	1.5
Magenta	0.50	2.0	1.5	2.0
Orange	0.50	2.0	1.5	1.0
Buff	0.38	1.5	1.5	1.5

OUTLINE DIMENSIONS

THERMAL INFORMATION

The maximum power consumption an integrated circuit can tolerate at a given operating ambient temperature can be found from the equation:

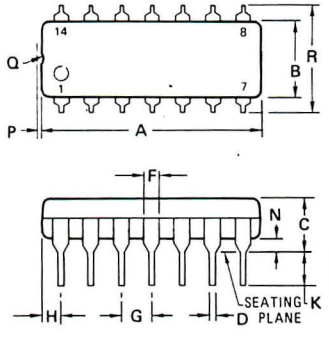
$$P_D(T_A) = \frac{T_{J(max)} - T_A}{R_{\theta JA}(typ)}$$

where $P_D(T_A)$ = Power Dissipation allowable at a given operating ambient temperature. This must be greater than the sum of the products of the supply voltages and supply currents at the worst-case operating condition.

$T_{J(max)}$ = Maximum Operating Junction Temperature as listed in the Maximum Ratings Section

T_A = Maximum Desired Operating Ambient Temperature

$R_{\theta JA}(typ)$ = Typical Thermal Resistance Junction to Ambient



P SUFFIX
PLASTIC PACKAGE
CASE 646-04
$R_{\theta JA}$ = 100°C/W Typical

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	18.03	19.56	0.710	0.770
B	6.10	6.60	0.240	0.260
C	–	5.08	–	0.200
D	0.38	0.53	0.015	0.021
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	1.32	2.41	0.052	0.095
J	0.20	0.38	0.008	0.015
K	2.92	–	0.115	–
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	–	0.020	–
R	–	8.26	–	0.325

NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
4. DIMENSION "R" TO BE MEASURED AT THE TOP OF THE LEADS (NOT AT THE TIPS).

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Appendix III

40-V Photo Darlington Transistors

MOTOROLA
SEMICONDUCTORS

MRD360
MRD370

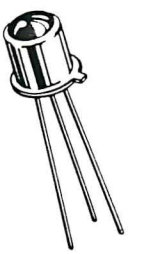
NPN SILICON HIGH SENSITIVITY PHOTO DARLINGTON TRANSISTORS

. . . designed for application in industrial inspection, processing and control, counters, sorters, switching and logic circuit or any design requiring very high radiation sensitivity at low light levels.

- Popular TO-18 Type Hermetic Package for Easy Handling and Mounting
- Sensitive Throughout Visible and Near Infra-Red Spectral Range for Wider Application
- Minimum Light Current 12 mA at H = 0.5 mW/cm^2 (MRD360)
- External Base for Added Control
- Switching Times –
  t_r @ I_L = 1.0 mA peak = 15 μs (Typ) – MRD370
  t_f @ I_L = 1.0 mA peak = 25 μs (Typ) – MRD370

40 VOLT
PHOTO DARLINGTON TRANSISTORS
NPN SILICON

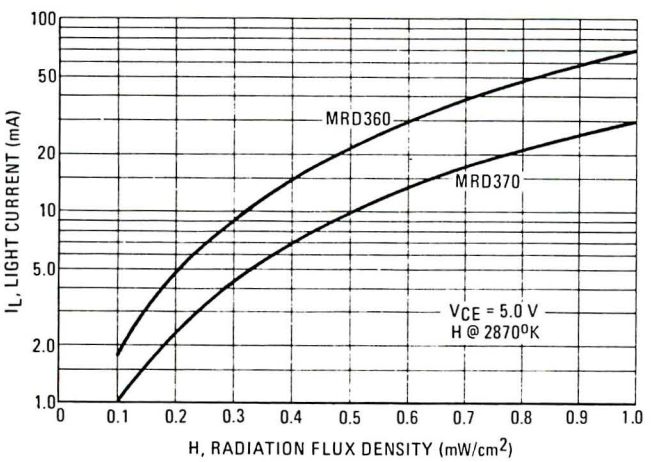
250 MILLIWATTS

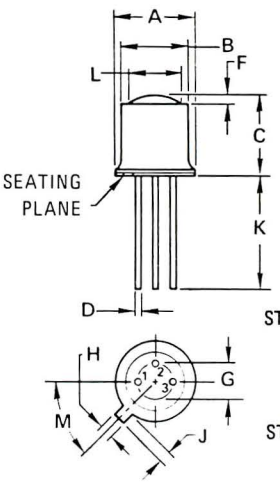


MAXIMUM RATINGS (T_A = 25°C unless otherwise noted).

Rating (Note 1)	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	40	Volts
Emitter-Base Voltage	V_{EBO}	10	Volts
Collector-Base Voltage	V_{CBO}	50	Volts
Light Current	I_L	250	mA
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	250 1.43	mW mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	°C

FIGURE 1 – LIGHT CURRENT versus IRRADIANCE





STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

STYLE 2:
PIN 1. CATHODE
2. GATE
3. ANODE

NOTES:
1. LEADS WITHIN .13 mm (.005) RADIUS OF TRUE POSITION AT SEATING PLANE, AT MAXIMUM MATERIAL CONDITION.
2. PIN 3 INTERNALLY CONNECTED TO CASE.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	5.31	5.84	0.209	0.230
B	4.52	4.95	0.178	0.195
C	5.08	6.35	0.200	0.250
D	0.41	0.48	0.016	0.019
F	0.51	1.02	0.020	0.040
G	2.54 BSC		0.100 BSC	
H	0.99	1.17	0.039	0.046
J	0.84	1.22	0.033	0.048
K	12.70	–	0.500	–
L	3.35	4.01	0.132	0.158
M	45° BSC		45° BSC	

CASE 82
TO-18

STATIC ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Collector Dark Current (V_{CE} = 10 V, H ≈ 0) T_A = 25°C	I_{CEO}	–	10	100	nA
Collector-Base Breakdown Voltage (I_C = 100 μA)	BV_{CBO}	50	–	–	Volts
Collector-Emitter Breakdown Voltage (I_C = 100 μA)	BV_{CEO}	40	–	–	Volts
Emitter-Base Breakdown Voltage (I_E = 100 μA)	BV_{EBO}	10	–	–	Volts

OPTICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristic	Device Type	Symbol	Min	Typ	Max	Unit
Light Current V_{CC} = 5.0 V, R_L = 10 Ohms (Note 1)	MRD360 MRD370	I_L	12 3.0	20 10	– –	mA
Collector-Emitter Saturation Voltage (I_L = 10 mA, H = 2 mW/cm^2 at 2870°K)		$V_{CE(sat)}$	–	–	1.0	Volts
Photo Current Rise Time (Note 2) (R_L = 100 ohms, I_L = 1.0 mA peak)	MRD360 MRD370	t_r	– –	40 15	100 100	μs
Photo Current Fall Time (Note 2) (R_L = 100 ohms, I_L = 1.0 mA peak)	MRD360 MRD370	t_f	– –	60 25	150 150	μs

NOTES:

1. Radiation flux density (H) equal to 0.5 mW/cm^2 emitted from a tungsten source at a color temperature of 2870 K.
2. For unsaturated response time measurements, radiation is provided by pulsed GaAs (gallium-arsenide) light-emitting diode ($\lambda \approx 0.9$ μm) with a pulse width equal to or greater than 500 microseconds (see Figure 6) I_L = 1.0 mA peak.

TYPICAL ELECTRICAL CHARACTERISTICS

FIGURE 2 – COLLECTOR-EMITTER SATURATION CHARACTERISTIC

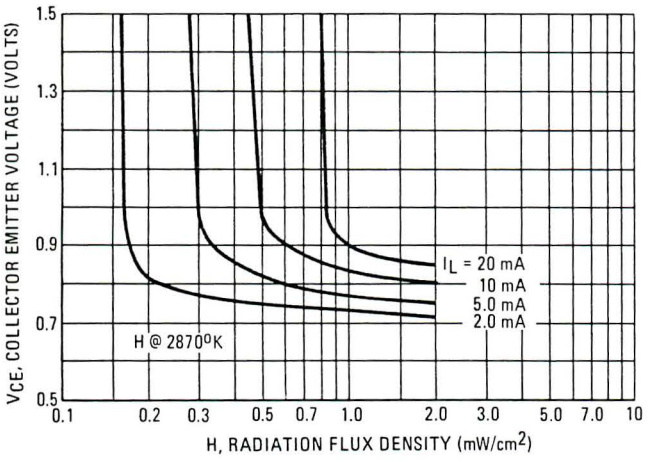


FIGURE 3 – COLLECTOR CHARACTERISTICS

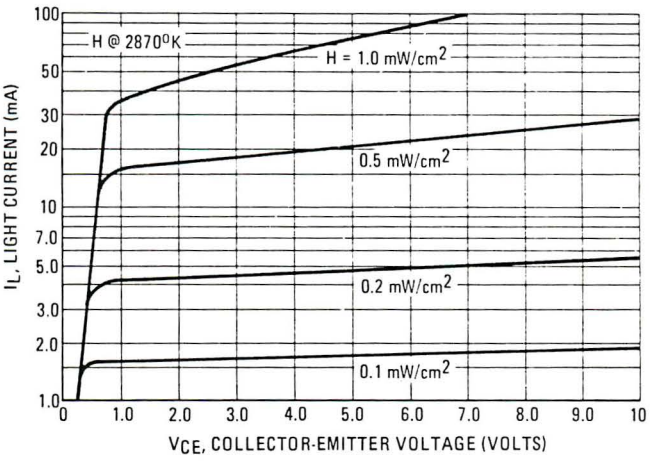


FIGURE 4 – NORMALIZED LIGHT CURRENT versus TEMPERATURE

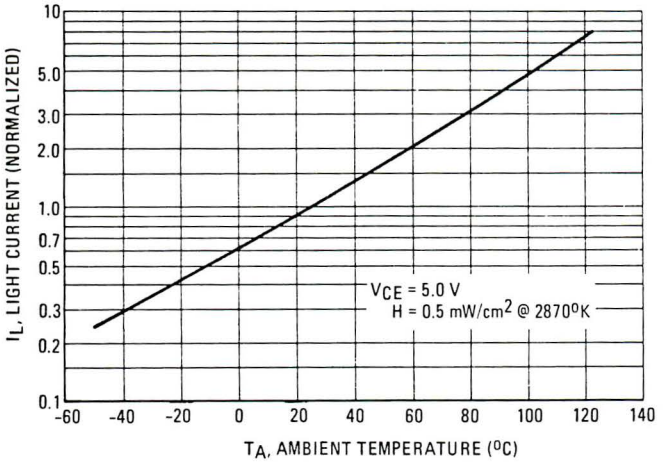


FIGURE 5 – DARK CURRENT versus TEMPERATURE

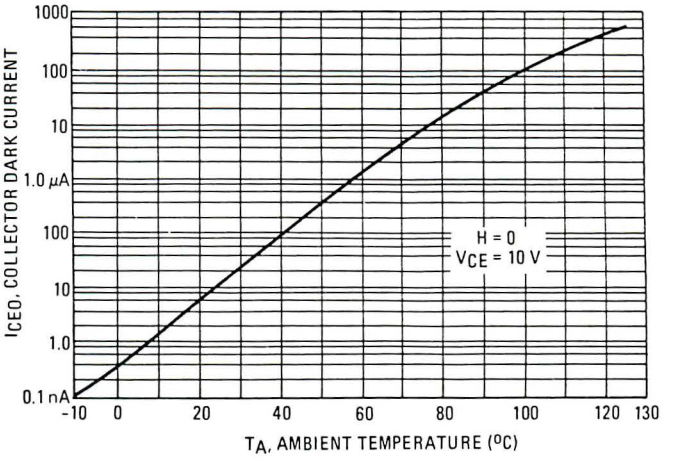
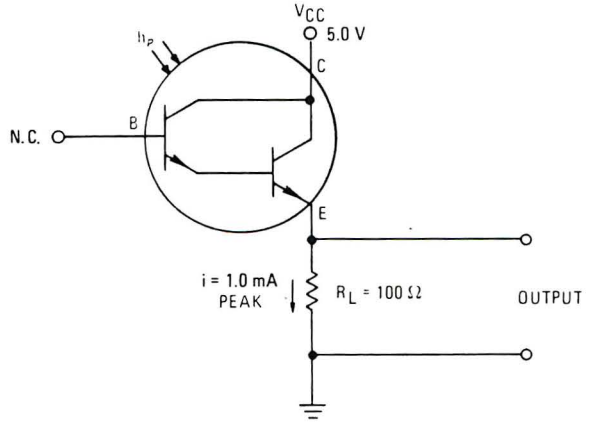


FIGURE 6 – PULSE RESPONSE TEST CIRCUIT AND WAVEFORM



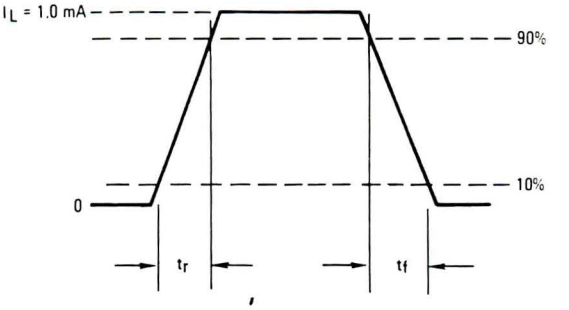


FIGURE 7 – CONSTANT ENERGY SPECTRAL RESPONSE

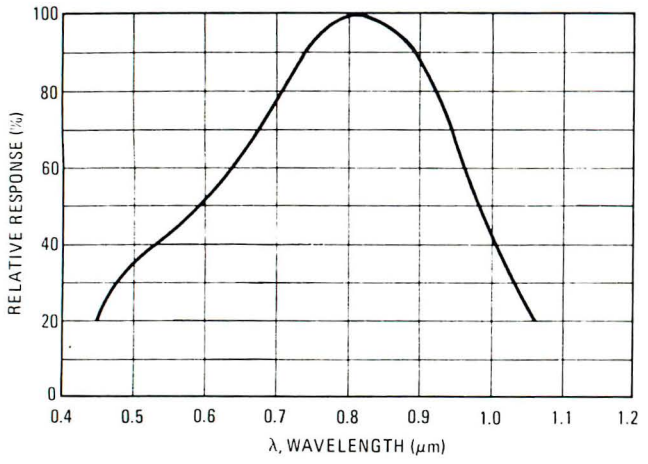
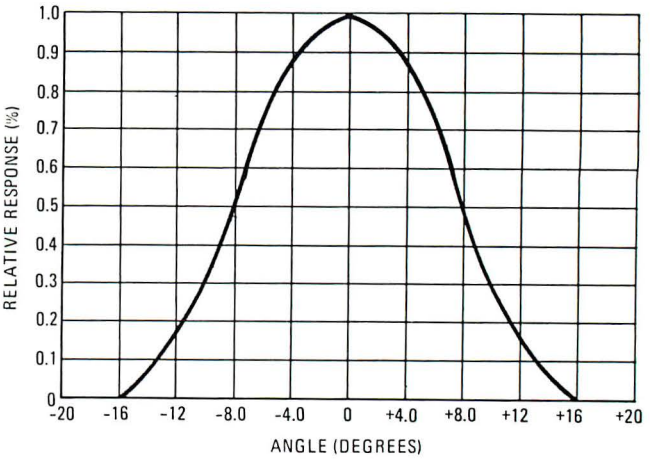


FIGURE 8 – ANGULAR RESPONSE



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AN-440 Theory and Characteristics of Photo Transistors

AN-508 Applications of Phototransistors in Electro-Optic Systems.

AN-561 How to Use Photosensors and Light Sources

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Appendix IV

System Aspects of the Motorola MC6847

SYSTEM ASPECTS OF THE MOTOROLA MC6847

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The integration of a sub-system on a single monolithic silicon die makes it increasingly difficult to supply all relevant design information in a concise data sheet. The need to supply support documentation to bridge the gap between the device electrical and timing specifications given in the data sheet and that of the system in which the device is to be used becomes apparent. The following paper fulfills this requirement for the Motorola MC6847 Video Display Generator (VDG).

There are two similar Video Display Generators on the market. However, they are neither pin compatible nor feature compatible. These are the S68047 from American Microsystems Incorporated and the MC6847 by Motorola Incorporated. The AMI VDG derives its T.V. system timing from a 3.58MHz clock and video timing from a separate RC clock, while the Motorola VDG derives all its timing from a single 3.58MHz master clock. The AMI luminance signal is basically digital--that is, presence or absence of video information--whereas, the Motorola luminance signal has three grey levels in addition to black. The AMI VDG is interlaced, while Motorola offers both interlaced and non-interlaced versions. In this report we deal only with the Motorola VDG.

The Motorola MC6847 VDG together with the MC1372 Video Modulator make up a miniature television transmitter, transmitting at 61.25MHz (Channel 3) or 67.25MHz (Channel 4) depending on component values chosen. This being a Class I T.V. device, care must be taken to meet F.C.C. requirements Part 15, Subpart H. If however, the composite video output from the MC1372 were to drive the television directly, Section 15.7 of the F.C.C. specification must be adheared to.

Television transmition in North and South America and Japan conform to the National Television System Committee (NTSC) standards. This system is based on a field repetition rate of 60 fields per second. Field duration is the reciprocal of the field rate (V=16.66mS). There are 525 interlaced lines per frame or one-half this number per field. At 60 fields per second, there are a total of 15,750 lines per second. Line duration is the reciprocal of the line rate (H=63.5uS). There is little agreement in the literature regarding the tolerance of the NTSC specifications [1], [2], [3]. Figures 1 and 2 tabulate the horizontal and vertical timing from three references. Fortunately, the television receiver is quite tolerant of deviations from the nominal values.

The horizontal timing for the VDG is summarized in Figure 3. Ten and one-half cycles of the 3.58MHz subcarrier is transmitted on the back porch of every horizontal blanking period. This colour sync burst is suppressed during vertical sync and equalizing intervals. Colour burst is also suppressed in the most dense two color graphic mode. This leads to some interesting rainbow effect on the display which is frequency and pattern dependent. The vertical timing for the VDG is given in Figure 4. Vertical retrace is initiated by the luminance signal being brought to blanking level. The vertical blanking period begins with three lines of equalizing pulses followed by three lines of serrated vertical sync pulses followed by three more lines of equalizing pulses. The remaining vertical blanking period contains the normal horizontal sync pulses. The equalizing and serration pulses are at half line frequency. Notice the difference in spacing between the last horizontal sync pulse and the first equalizing pulse in even and odd fields. It is this half line difference between fields that produces the interlaced picture in a frame. Vertical timing between fields for the non-interlaced VDG, on the other hand, is identical. The equalizing and serration pulses are, however, at line frequency.

For compatible colour transmition the NTSC has established the relationship of the luminance level to the red, green and blue levels as given in Equation 1. Consequently, the colour difference signals are of the form in Equation 2 and 3.

$$Y = 0.30R + 0.59G + 0.11B \quad (1)$$

$$R-Y = 0.70R - 0.59G - 0.11B \quad (2)$$

$$B-Y = -0.30R - 0.59G + 0.89B \quad (3)$$

The sync to video ratio of the total luminance level is 25% and 75% respectively. Reference white level is 10% to 15%. The relative magnitude of luminance and chromanance signals are given in Figure 5a. for a colour bar of 100% colour saturation. The same colour bar with its associated colour levels are given in Figure 5b for the VDG. A comparison of these figures show that certain liberties have been taken to trade off hue and intensity fidelity for chip simplicity. That is, the seven luminance grey levels have been reduced to three and six chromanance levels have been reduced to two.

Recalling that all timing in the Motorola VDG is generated from the 3.58MHz master clock, the total horizontal screen span from blanking to blanking is 185.5 periods of this clock, or approximately 51.82μS. The display window is offset from the left hand edge by 29.5 periods and lasts for 128 periods or 35.76μS. Of the 242 lines on the vertical screen from blanking to blanking, 192 lines are used for the display. The display window is offset from the top by 25 lines. These relationships are depicted in Figure 6. Under the constraint of the master clock, the smallest display element possible for the VDG is half period of the 3.58MHz clock wide by one scan line high. All other display elements are multiples of this basic size. For a 19 inch diagonal T.V. screen the display window corresponds to approximately 26cm by 22cm and the smallest element is about 1mm by 1.14mm high.

There are two major display modes in the VDG. Major mode 1 contains four alphanumeric and two limited graphic modes. Major mode 2 contains eight graphic modes. Of these, four are full colour graphic and four restricted colour graphic modes. The mode selection for the VDG is summarized in Figure 7. The mneumonics of these fourteen modes are explained in the following sections.

In major mode 1 the display window is divided into 32 columns by 16 character element rows. Each character element is 8 half periods by 12 scan lines in size. The area outside the display window is black.

The VDG has a built-in character generator ROM containing the 64 ASCII characters in a 5x7 format. The 5x7 character font is positioned two columns to the right and three rows down within the 8x12 character element. For those who wish to display lower case letters, special characters, or even limited graphic an external ROM can be used. If such external ROM is used, all of the 8x12 picture elements, or pictels, in the character element can be utilized. Video inversion can be effected to either illuminate the pictels defining the character leaving the background black (non-inverted), or darken the character pictels and illuminating the background (inverted). The four alphanumeric modes are, then, internal non-inverted alphanumeric (INA), internal inverted alphanumeric (IIA), external non-inverted alphanumeric (ENA), and external inverted alphanumeric (EIA).

The two limited graphic modes are semigraphic-4 (SG4) and semigraphic-6 (SG6). In SG4, the character is divided into four 4x6 pictels. Similarly, the character element in SG6 is divided into six 4x4 pictels. In the semigraphic modes, three bits of input data choose one of eight colours for the whole character element. The low order four or six data bits are used as illumination data in SG4 and SG6 respectively. If the illumination bit is high the pictel is illuminated. If it is low the pictel is black. The mapping of data input bits to the display formats and the colour selection are given in Figure 8.

The display window in major mode 2 has a less rigorous format than in major mode 1. The display elements vary from one scan line to three scan lines in height. The length of the display element is either eight or sixteen half periods wide. Each display element is divided into four or eight pictels. The former corresponds to a full colour mode while the latter a restricted colour mode. Each data bit in the restricted colour mode, like the semigraphic modes, represents illumination data. When it is high the pictel is illuminated with the colour chosen by the Colour Set Select (CSS) pin. When it is low the pictel is black. In the full colour modes, pairs of data bits choose one of four colours in one of two colour sets defined by the CSS pin. Depending on the state of the CSS pin, the area outside the display window is either green or buff. The display formats and colour selection for this major mode are summarized in Figure 9.

The block diagram in Figure 10 shows how the VDG is related to other functional blocks in a typical system. A negative Row Preset signal ($\overline{RP}$) generated by the VDG initializes the row scan counter for the external character generator once every twelve scan lines, while the negative Horizontal Sync ($\overline{HS}$) acts as clock to this counter. The negative Field Sync ($\overline{FS}$) generates an interrupt to the MPU, signifying that the display memory can be updated without interference with the VDG display function. This signal must not be confused with the system vertical sync signal. Field Sync is activated by the end of the vertical display window and deactivate by the trailing edge of vertical sync. This gives the MPU a total of thirty-two scan lines or 2.03mS to update the display memory. The MPU acknowledges the interrupt request from the VDG by bringing the negative Memory Select input ($\overline{MS}$) to the VDG low. This puts the address bus output from the VDG

into high impedence state, thus relinquishing bus control to the MPU. The timing relationship of Horizontal Sync, Row Preset, and Field Sync are given in Figure 11.

The display memory is an element by element map of the display window on the screen. The VDG addresses the display memory storage locations in succession and translates their contents into luminance and chromanance levels. The frequency of address update is dependent on the length of the display element. Recall that display elements in major mode 1 are four periods and major mode 2 are either four or eight periods of the master clock. Data from the display memory is latched on every address transition. Hence, the data for the first display element must be stable four or eight periods before the horizontal display window depending on the display mode selected. This timing requirement is illustrated in Figure 12.

Examination of Figures 8 and 9 reveals that all display elements within major mode 1 are similar while that within major mode 2 are largely dissimilar. Therefore, mode switching between alphanumeric modes and semi-graphic modes can be carried out freely. Care must be taken, however, when performing mode switching in major mode 2. The only compatible modes are between CG1 and RG1, and between CG6 and RG6. Minor mode switching within the same major mode in a given element row can be achieved as long as it is between compatible modes. It should be quite apparent that major mode switching on an element by element basis is impractical. It can be achieved, however, at the expense of added component count. The element formats in the VDG lend themselves to major mode switching between element rows. The presence of Row Preset in major mode 1 serves as a flag for the beginning of a new element row. Detection of this signal can initiate a major mode switch from 1 to 2.

Display memory size is a function of the display density. Quite often a graphic display contains shapes that are several times larger than that of the display elements in the VDG. This is particularly true of certain video games. Much of the display consists of a fixed background. The vertical size of a display element can be doubled or quadrupled by simply ignoring the lowest order or the first two low order vertical addresses respectively from the VDG. Reduction of address lines naturally lead to reduction in memory size. Another method of memory reduction is to store objects or object fragments in

ROM and store their display addresses in the RAM portion of display memory. Here, the larger the object fragment, the greater the memory saving.

Timing and signal levels of the Motorola VDG have been related to system timing and signal levels as specified by the NTSC. Salient features of display formats are discussed and cautions to their application pointed out. Some system configurations have been suggested as illustrations of efficient usage.

References

1. Harold E. Ennes
   Television Broadcasting Equipment,
   Systems, and Operating Fundamentals
   Howard W. Sams, 1971.

2. Bernard Grob
   Basic Television Principles and Servicing
   McGraw-Hill, 1975

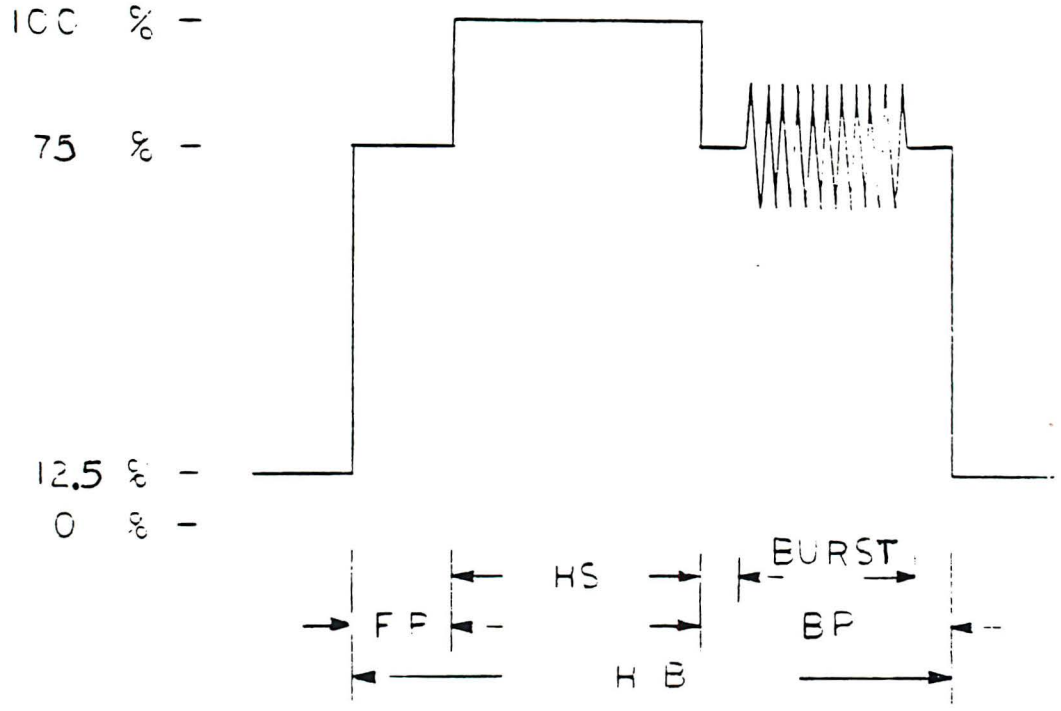
3. W. Wharton and D. Howorth
   Principles of Television Reception
   Pitman Press, 1967

TIMING LIMIT	REFERENCE			
	ENNES[1]	GROB[2]	WHARTON & HOWORTH[3]	UN
HORIZONTAL BLANKING	11.1 $^{+\ 0.3}_{-\ 0.6}$	10.16 $\pm$ 1.27	10.8 (MIN)	US
HORIZONTAL SYNC	4.76 $\pm$ 0.32	5.08	4.85 $\pm$ 0.65	US
FRONT PORCH	1.38 $^{+\ 0.13}_{-\ 0.32}$	1.27	1.7 (MIN)	US
BACK PORCH	4.76 $^{+\ 0.96}_{-\ 0.61}$	3.81	4.25 $\pm$ 0.65	US
SYNC TO BURST	0.56 $^{+\ 0.08}_{-\ 0.17}$			US
BURST	2.24 $^{+\ 0.27}_{-\ 0.0}$			US

FIGURE 1. NTSC HORIZONTAL TIMING SPECIFICATION

TIMING LIMIT	REFERENCE		
	ENNES[1]	GROB[2]	WHARTON & HOWORTH[3]
VERTICAL BLANKING	18.375H TO 21H	0.05V TO 0.08V	(13H TO 21H)+H BLANKING
LEADING EQUALIZING PULSES		3H	3H
V BLANKING TO V SYNC	3.02 $^{+1}_{-0}$ H		
VERTICAL SYNC	3H	3H	3H
TRAILING EQUALIZING PULSES		3H	3H
BURST BLANKING	9H	9H	

FIGURE 2. NTSC VERTICAL TIMING SPECIFICATION

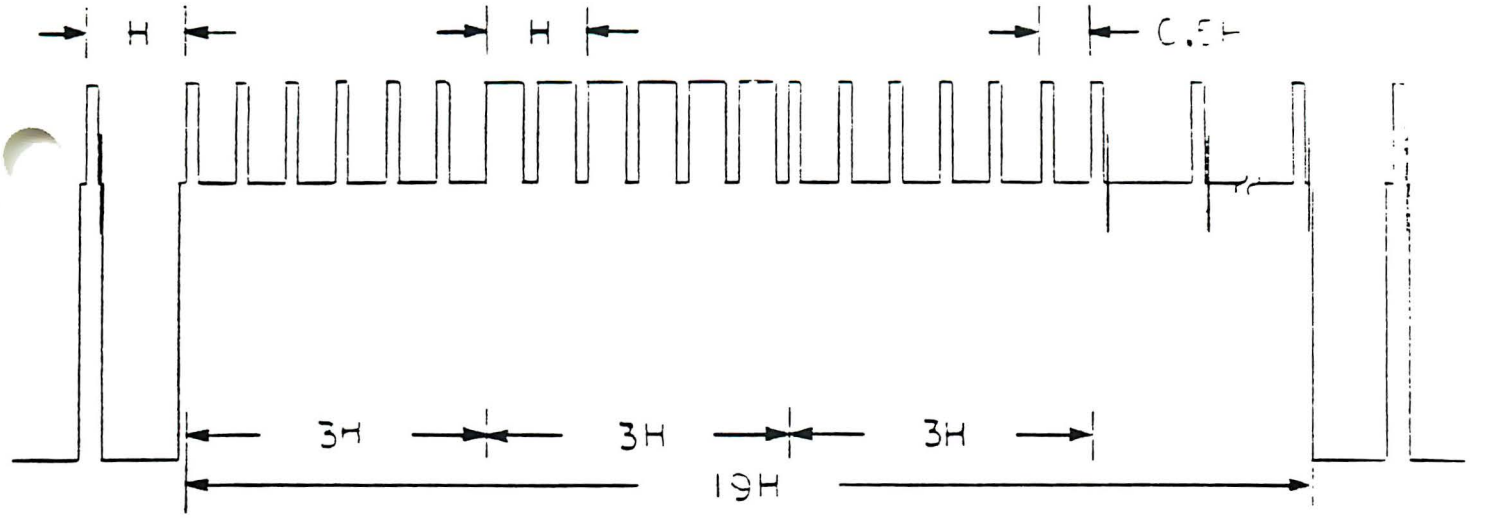


(a) COMPOSITE WAVEFORM

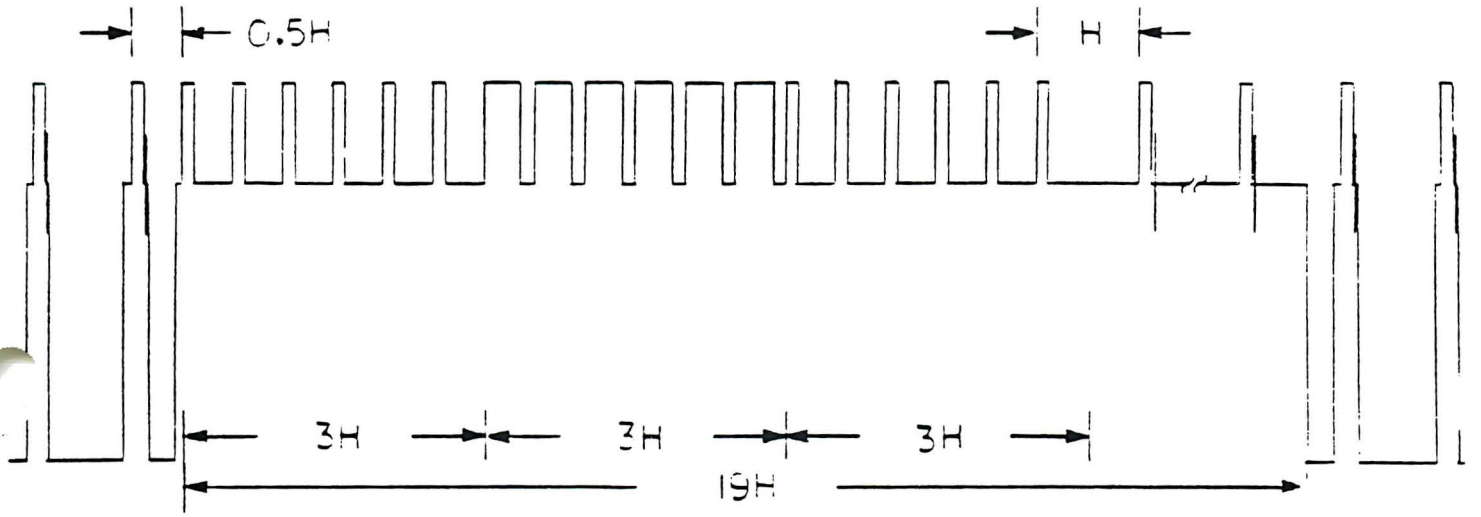
HORIZONTAL BLANKING	11.733	µS
HORIZONTAL SYNC	4.888	µS
FRONT PORCH	1.955	µS
BACK PORCH	4.888	µS
BURST	2.933	µS
SYNC TO BURST	0.977	µS

(b) NOMINAL CHIP VALUES

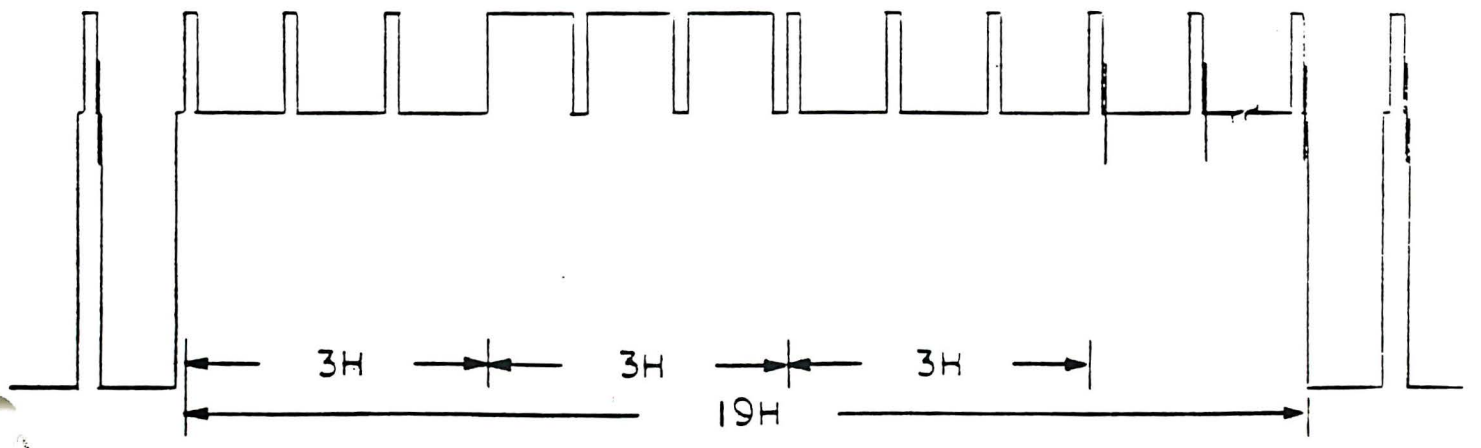
FIGURE 3. VDG HORIZONTAL TIMING



(a) EVEN FIELD INTERLACED

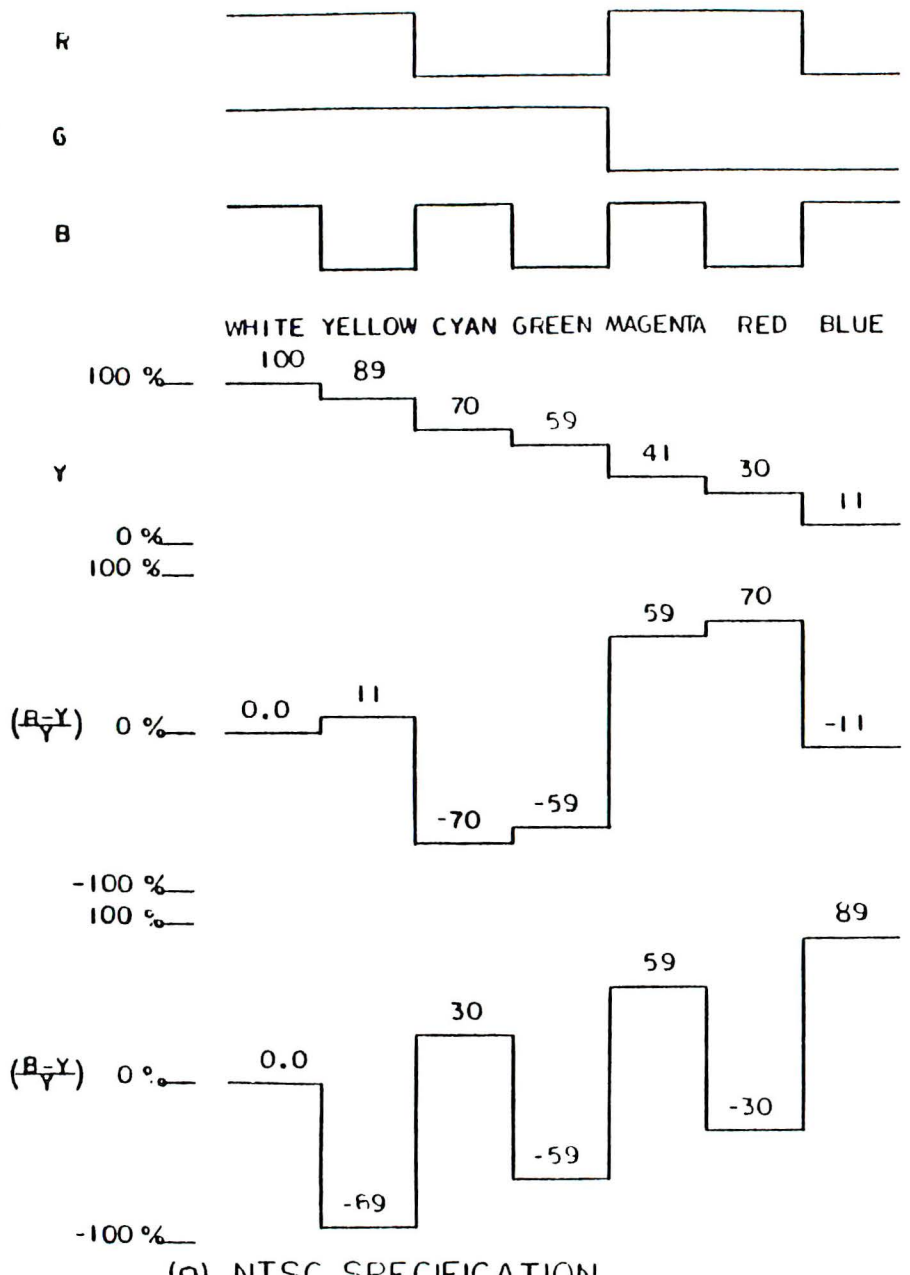


(b) ODD FIELD INTERLACED

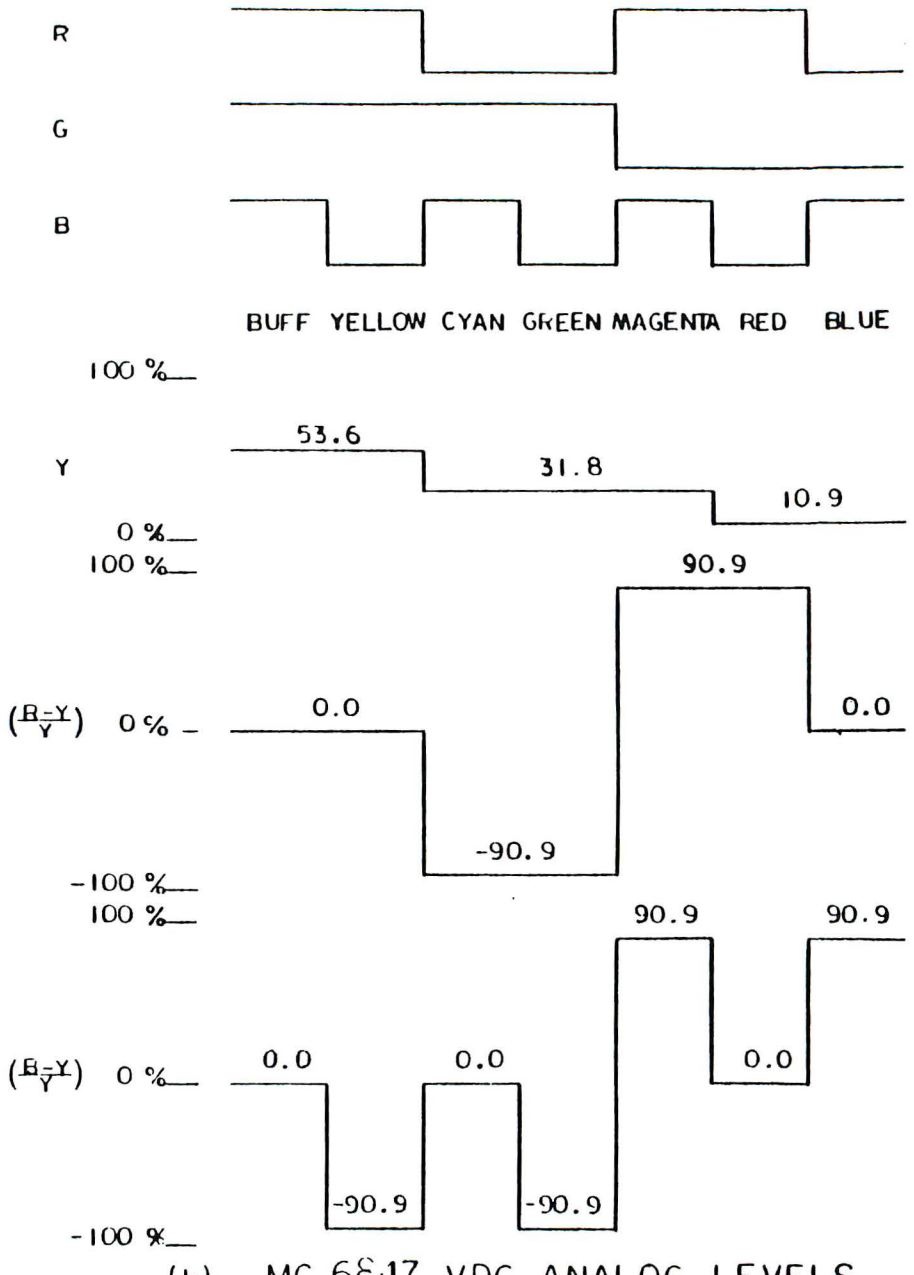


(C) EVEN/ODD FIELD NON-INTERLACED

FIGURE 4. VDG VERTICAL TIMING



(a) NTSC SPECIFICATION



(b) MC 6847 VDG ANALOG LEVELS

FIGURE 5. PERCENTAGE LUMINANCE FOR COLOUR BAR

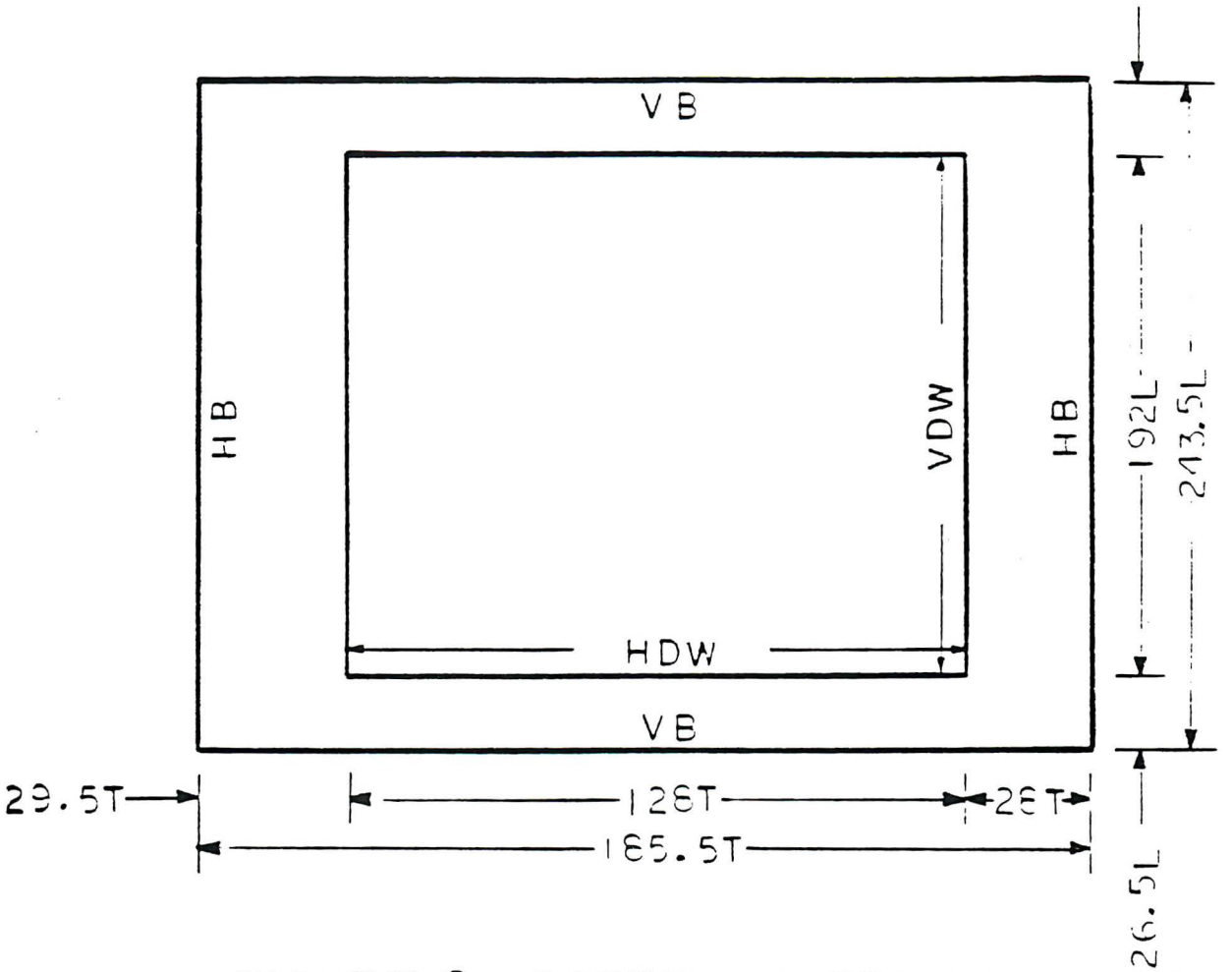
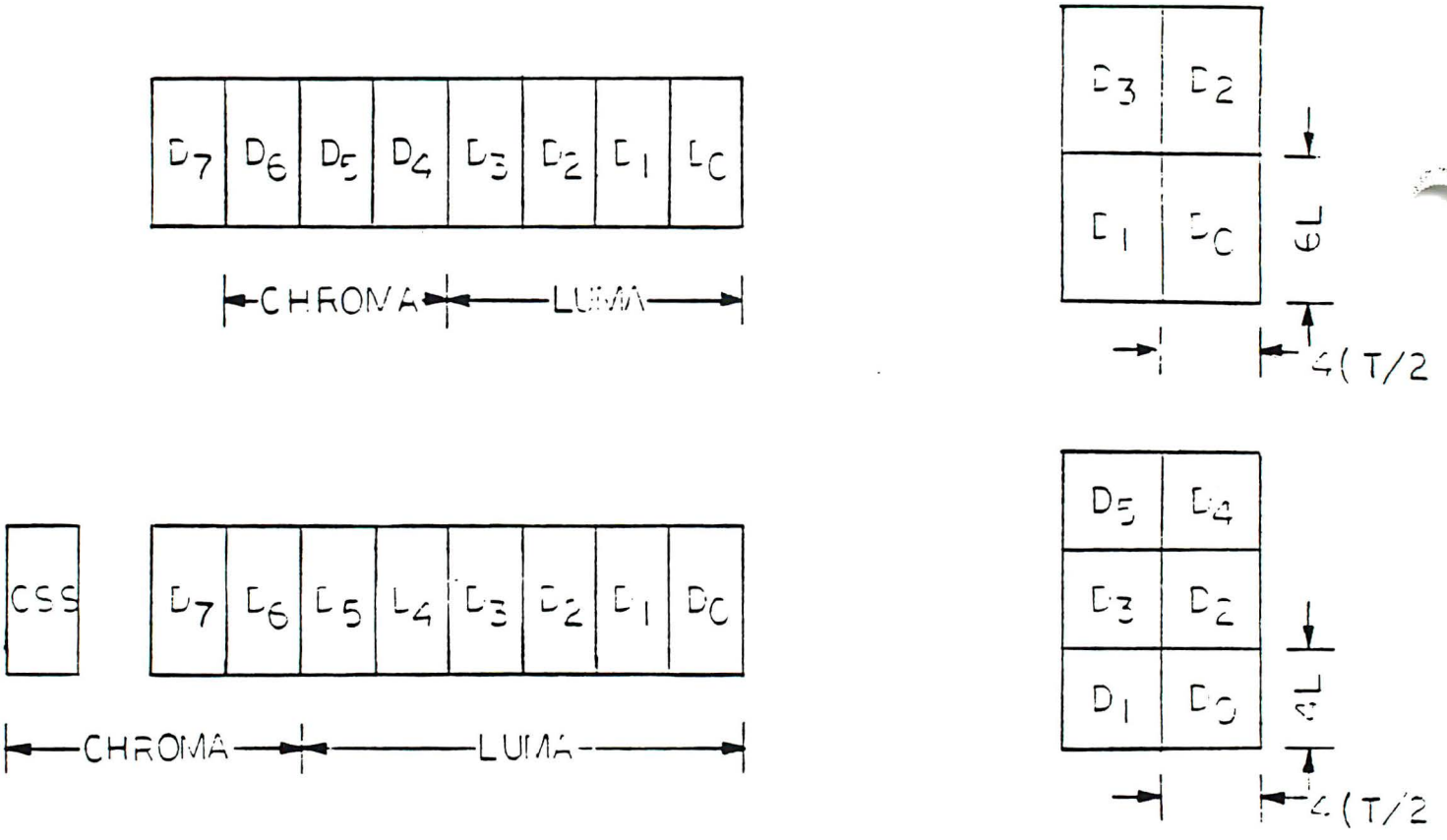


FIGURE 6. SCREEN DISPLAY WINDOW

A/G	T/S	I/E	INV	GM2	GM1	GM0	MODE
0	0	0	0	X	X	X	INA
0	0	0	1	X	X	X	IIA
0	0	1	0	X	X	X	ENA
0	0	1	1	X	X	X	EIA
0	1	0	X	X	X	X	SG4
0	1	1	X	X	X	X	SG6
1	X	X	X	0	0	0	CG1
1	X	X	X	0	0	1	RG1
1	X	X	X	0	1	0	CG2
1	X	X	X	0	1	1	RG2
1	X	X	X	1	0	0	CG3
1	X	X	X	1	0	1	RG3
1	X	X	X	1	1	0	CG6
1	X	X	X	1	1	1	RG6

X: DON'T CARE STATE.

FIGURE 7. MC6847 MODE SELECTION

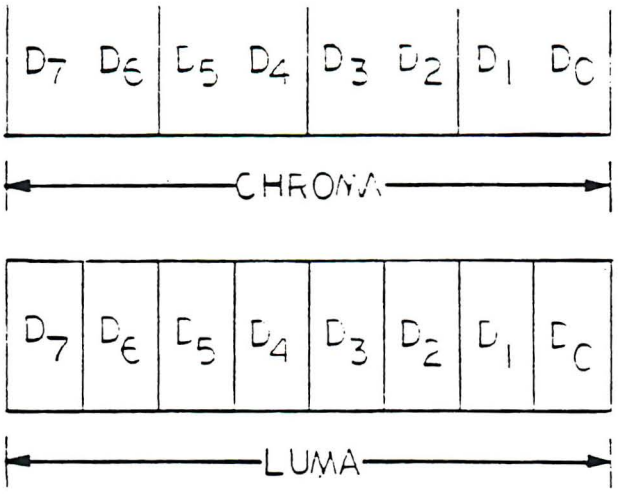


(a) DATA AND DISPLAY FORMATS

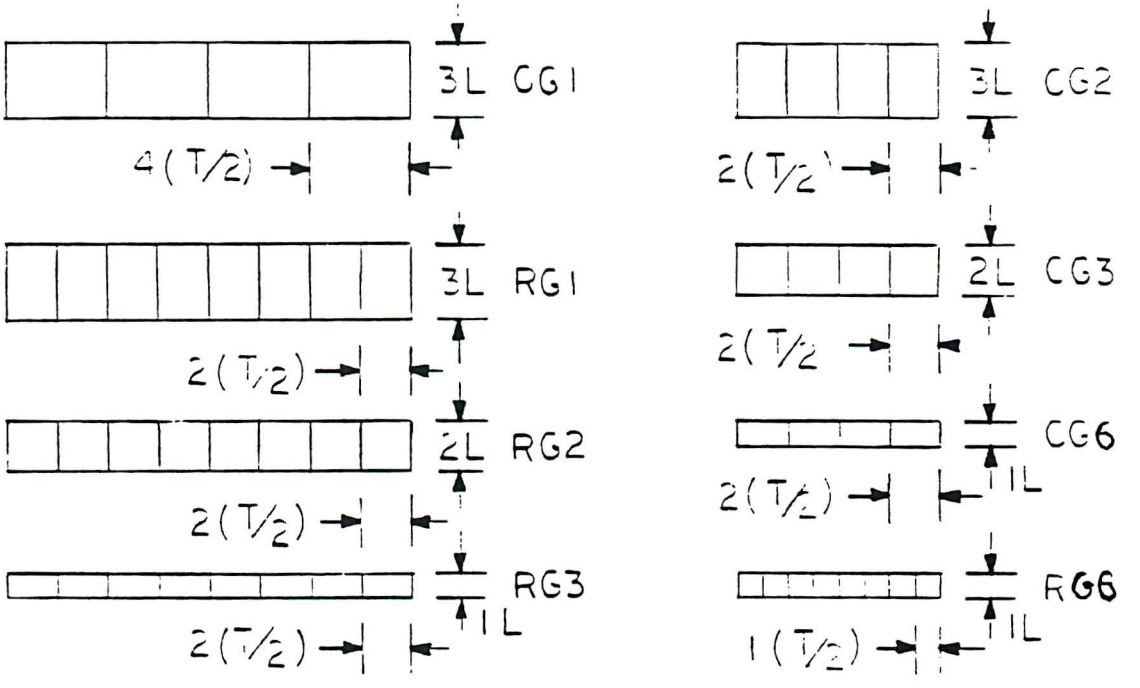
LUMA D_N	SG4			SG6			COLOUR
	D_6	D_5	D_4	CSS	D_7	D_6	
0	X	X	X	X	X	X	BLACK
1	0	0	0	0	0	0	GREEN
1	0	0	1	0	0	1	YELLOW
1	0	1	0	0	1	0	BLUE
1	0	1	1	0	1	1	RED
1	1	0	0	1	0	0	BUFF
1	1	0	1	1	0	1	CYAN
1	1	1	0	1	1	0	MAGENTA
1	1	1	1	1	1	1	ORANGE

(b) COLOUR SELECTION

FIGURE 8. SEMIGRAPHIC MODE ENCODING



(a) DATA FORMAT



(b) DISPLAY FORMAT

CSS	BORDER	RESTRICTED COLOUR MODE		COLOUR MODE		
		D_N	COLOUR	D_{N+1}	D_N	COLOUR
0	GREEN	0	BLACK	0	0	GREEN
0	GREEN	1	GREEN	0	1	YELLOW
0	GREEN	1	GREEN	1	0	BLUE
0	GREEN	1	GREEN	1	1	RED
1	BUFF	0	BLACK	0	0	BUFF
1	BUFF	1	BUFF	0	1	CYAN
1	BUFF	1	BUFF	1	0	MAGENTA
1	BUFF	1	BUFF	1	1	ORANGE

(C) COLOUR SELECTION

FIGURE 9. GRAPHIC MODE ENCODING

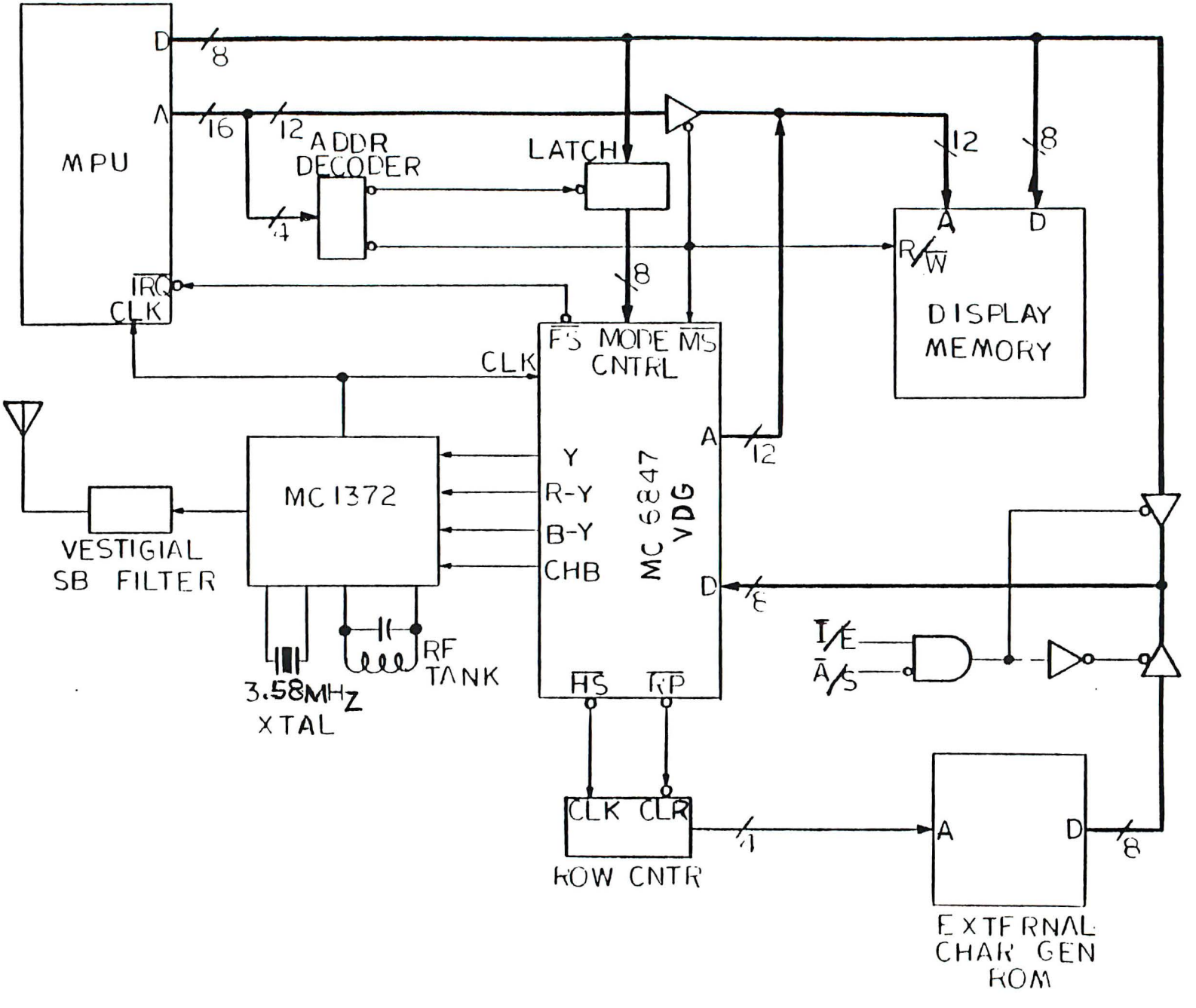
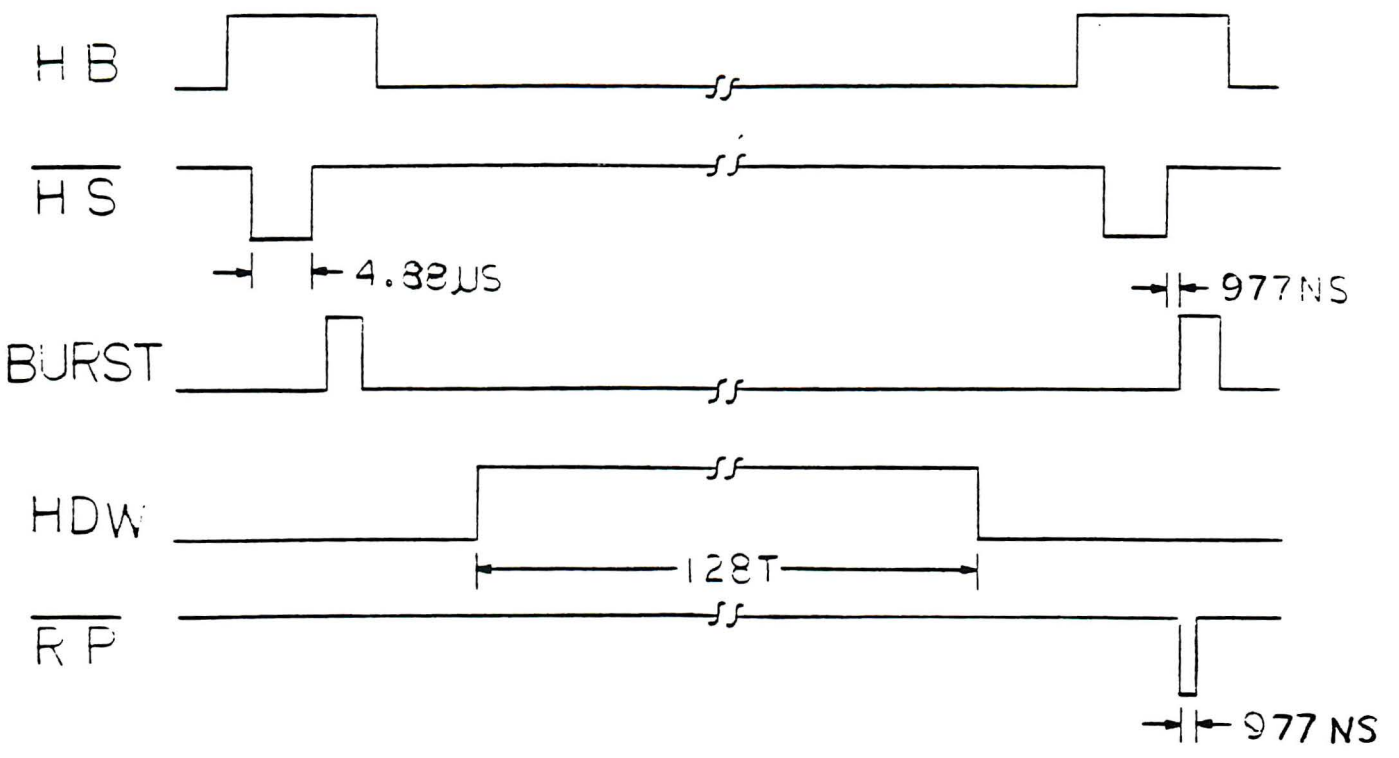
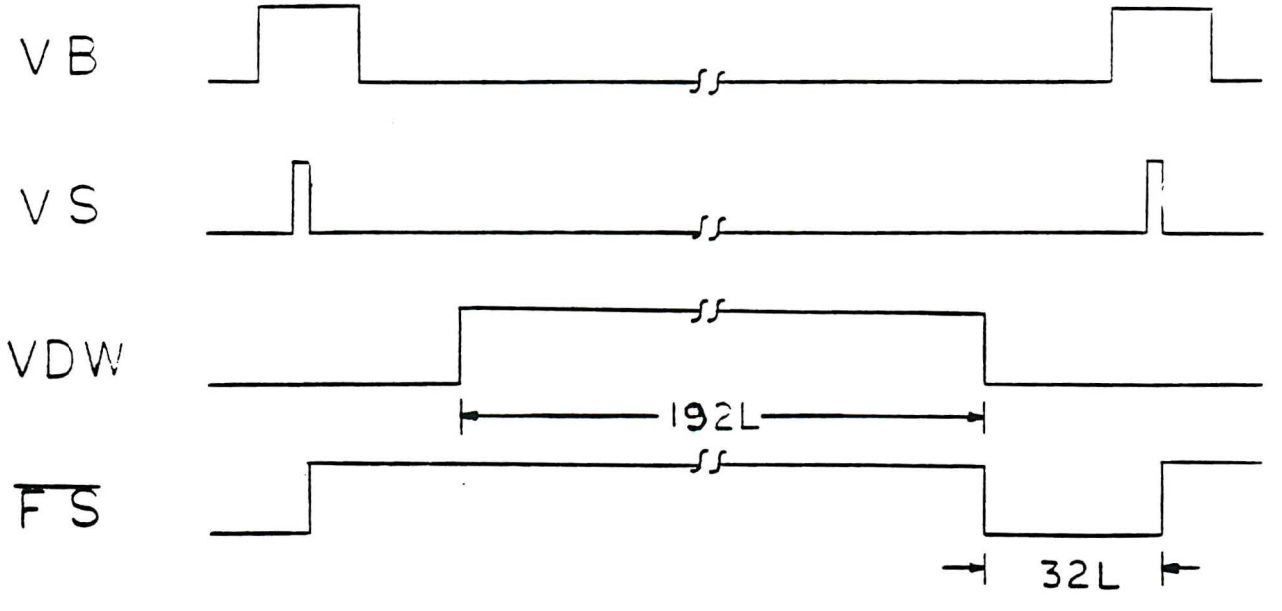


FIGURE IC. TYPICAL VDG SYSTEM

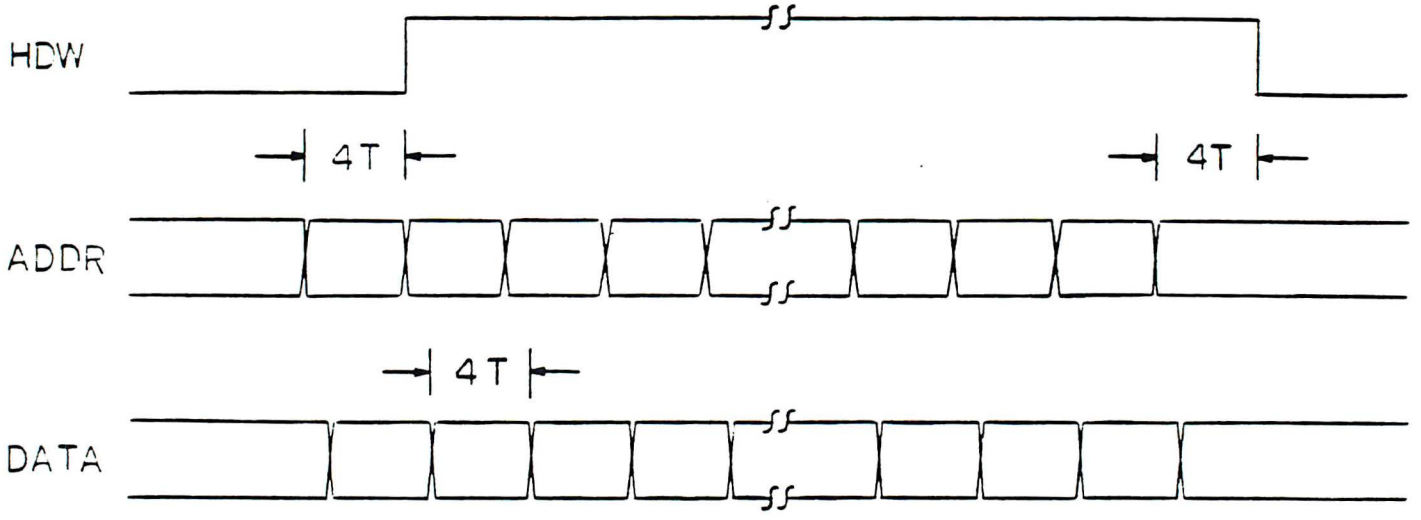


(a) HORIZONTAL TIMING

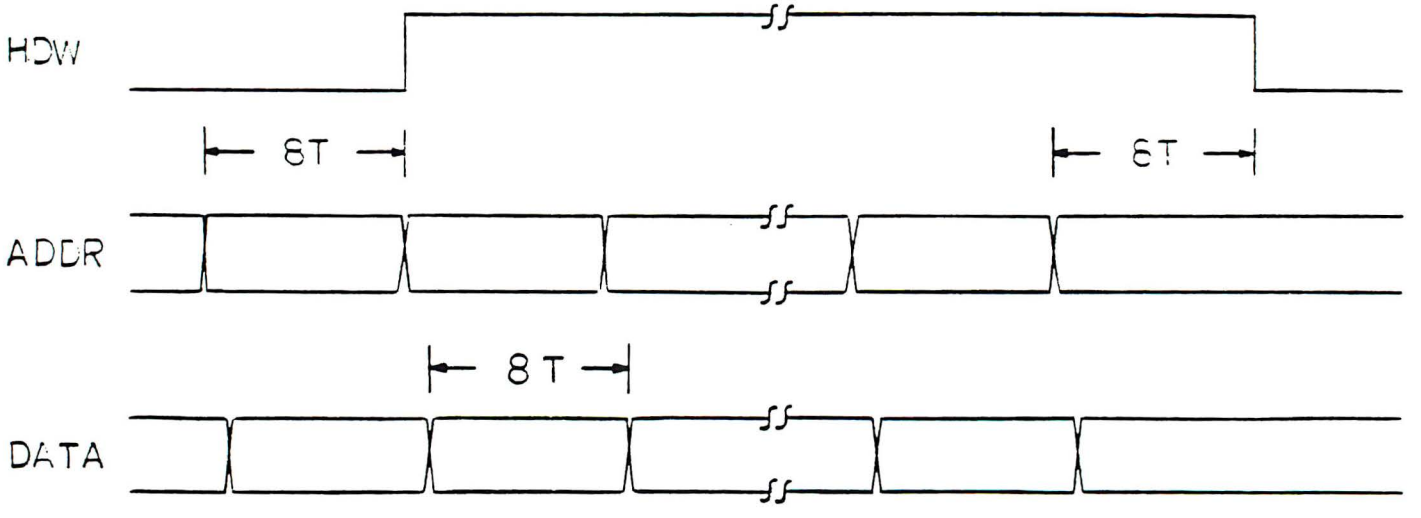


(b) VERTICAL TIMING

FIGURE 11. VGD SYSTEM INTERFACE TIMING



(a) SHORT ELEMENT MODE TIMING



(b) LONG ELEMENT MODE TIMING

FIGURE 12. VDG DATA INTERFACE TIMING

Appendix V

Adapting the MC6847 for Use With 625-Line, 50-Hz Receivers

1.0 INTRODUCTION

The MC 6847 video display generator (V.D.G.) is designed to generate 525 line, 60 Hz video signals. The output is in the form of a luminance signal and two colour difference signals, one of which includes a pulse for generating a colour subcarrier burst, thus corresponding to the Q axis of the N.T.S.C. system, while the other corresponds to the I axis. As european receivers are designed for 625 line, 50 Hz video and P.A.L. or S.E.C.A.M. colour, some considerable adaptation is required to produce a compatible system.

2.0 SCAN RATE CORRECTION

The line periods of the American and European systems are very similar. It is therefore sufficient to add 100 blank lines to the picture, the result being 625 lines, 50.4 Hz which is well within the locking range of a normal receiver. As it has the correct number of lines this signal is also compatible with count-down synchronisation systems. The inserted signal need only contain synchronisation and blanking levels, and can therefore be generated with simple logic circuitry. The arrangement is shown in fig. 1.

The V.D.G. has associated with it two signals which are utilised, $\overline{FS}$ goes low at the end of the active picture period and high at the end of the vertical sync. pulse. The 3.58 MHz N.T.S.C. subcarrier frequency is used as a clock for the V.D.G. The additional logic is basically a counter chain as follows: Four D flip-flops (74LS74) divide the clock by 2-1/2. There follow two synchronous counters with synchronous reset (74LS163), the first dividing by 7 to produce the line synchronisation period and the second dividing by 13 to produce the line period. A further D flip-flop is used at the output to provide synchronous positive and negative outputs. There follow two 74LS290 ripple counters connected as a divide by 50 counter with symetrical mark/space output. The output of these is exclusive ored with $\overline{FS}$ and fed to a 74LS74 D flip-flop connected with two nand gates as a clock stearing circuit. This directs the clock signal either to the V.D.G. or to the input of the counter chain, the change of path being determined by any change of state at the exclusive or input: Suppose that the V.D.G. is coming to the end of its active picture period with $\overline{FS}$ high. When $\overline{FS}$ goes low the clock signal is "stolen" from the V.D.G. which stops with the Y output at synchronisation level and the colour difference outputs at zero. The clock is fed to the counter chain which runs until a change of state occurs at the÷50 output, when the counter is stopped and the V.D.G. restarted. After the first attempt at insertion the system is self-phasing and on the second and subsequent insertions it generates a band of 50 lines on each side of the $\overline{FS}$ pulse, that is to say one at the top and one towards the bottom of the picture. Allowing the counter to "start where it left off" ensures that exactly the right number of clock periods are added to the frame time and avoids the accumulation of phase errors between the V.D.G. output and the inserted signal.

3.0 CONNECTION TO THE RECEIVER

Three possible forms of interface to the receiver may be considered:

a. R.G.B. signals

If the receiver is designed to accept R.G.B. input this will probably be in the form of three standard 1 volt, 75 ohm video signals, with synchronising pulses on at least 1 channel. This can be achieved using an emitter follower to buffer each output of the V.D.G., resistive matrixing and three 75 Ω line drivers. A level comparator referenced to the 5V supply to the V.D.G. would ensure that full amplitude synchronising signals were passed through to each output. Refer to figure 3.

b. Composite Video

A receiver designed for composite video input would again accept standard 1 volt, 75 Ω signals. In this case the buffered colour difference outputs of the V.D.G. must be modulated onto the appropriate sub-carrier, which signal is then added to the luminance, the whole being output through a 75 Ω line driver.

c. R.F. Input

In the event of a receiver not being equipped to accept a base-band input the only available interface is via the aerial socket. The solution here is as for composite video but instead of a 75 ohm line driver an r.f. modulator is required.

In order to demonstrate the achievable picture quality and solutions to the major problems, it was decided to design an adapter for P.A.L. composite video.

This also demonstrates a 75 Ω line driver suitable for the R.G.B. solution (which is, incidentally, guaranteed to give excellent picture quality). A major objective in this design was to eliminate adjustments as follows:

a. If the load impedance for the crystal is well enough defined, a crystal oscillator should run within the locking range of most decoders without a frequency adjusment.
b. A synthetic video signal is being handled and colour rendering is therefore not a problem. Further the hues are well differentiated. Precise quadrature of the modulation axes is not therefore required and, as the P.A.L. system averages two adjacent lines, neither is precise equality of + (R - Y) and - (R - Y) signal amplitudes. Finally all the colours generated are of high saturation, so that slight background tint is not important. Modulator carrier balance can therefore be omitted.

The circuit of the P.A.L. adapter is shown in fig. 2. The oscillator resonates the 4.43 MHz crystal in series with its load capacitance and gives antiphase outputs which are fed alternatively to the R-Y modulator by CMOS analogue gates (MC 14066) controlled by a CMOS flip-flop (MC 14013). The quadrature drive to the B - Y modulator is derived by a series RC time constant across the oscillator outputs and a resistive potential divider in the same position provides a d.c. reference for the carrier drive of the two modulators. The V.D.G. provides two colour difference signals plus a zero level voltage reference. These are buffered by emitter followers and fed directly to the modulators. A burst pulse only appears in the B-Y output of the V.D.G. and in order to generate P.A.L. modulation it is nececessary to scale its amplitude by $1/\sqrt{2}$ and inject this same amplitude to the reference feed to the R - Y modulator. This is done by means of R22, R23 and a further analogue gate from the MC 14066, which is controlled by a pulse which also clocks the flip-flop.

The pulse for controlling the burst generation and the flip-flop is derived from the horizontal pulse train by means of a transistor (essential for 5 V - 12 V interface) and the fourth analogue gate of the MC 14066. The back edge of the pulse lies between the trailing edge of the burst and that of the back porch. It has been found that some attention is necessary to the timing of the leading edge of this pulse. In most P.A.L. decoders the burst gate pulse leading edge is very close to the trailing edge of the synchronising pulse. Certain decoders are very sensitive to chroma frequency transients within the burst gate period and may refuse to unkill if these occur. The pulse is therefore timed to start about half-way through the synchronising pulse in order to avoid this problem, in preference to timing from the back edge of the sync. pulse.

The two modulators are type MC 1496. Their outputs are connected in parallel, R-C filtered and fed as a signal current to a summing node at the input of the 75 Ω line driver. Also added at this point are the mixed video signals, converted to a current signal, with the d.c. level preserved by reference to the 5 V rail so as to optimise the working point of the line driver.

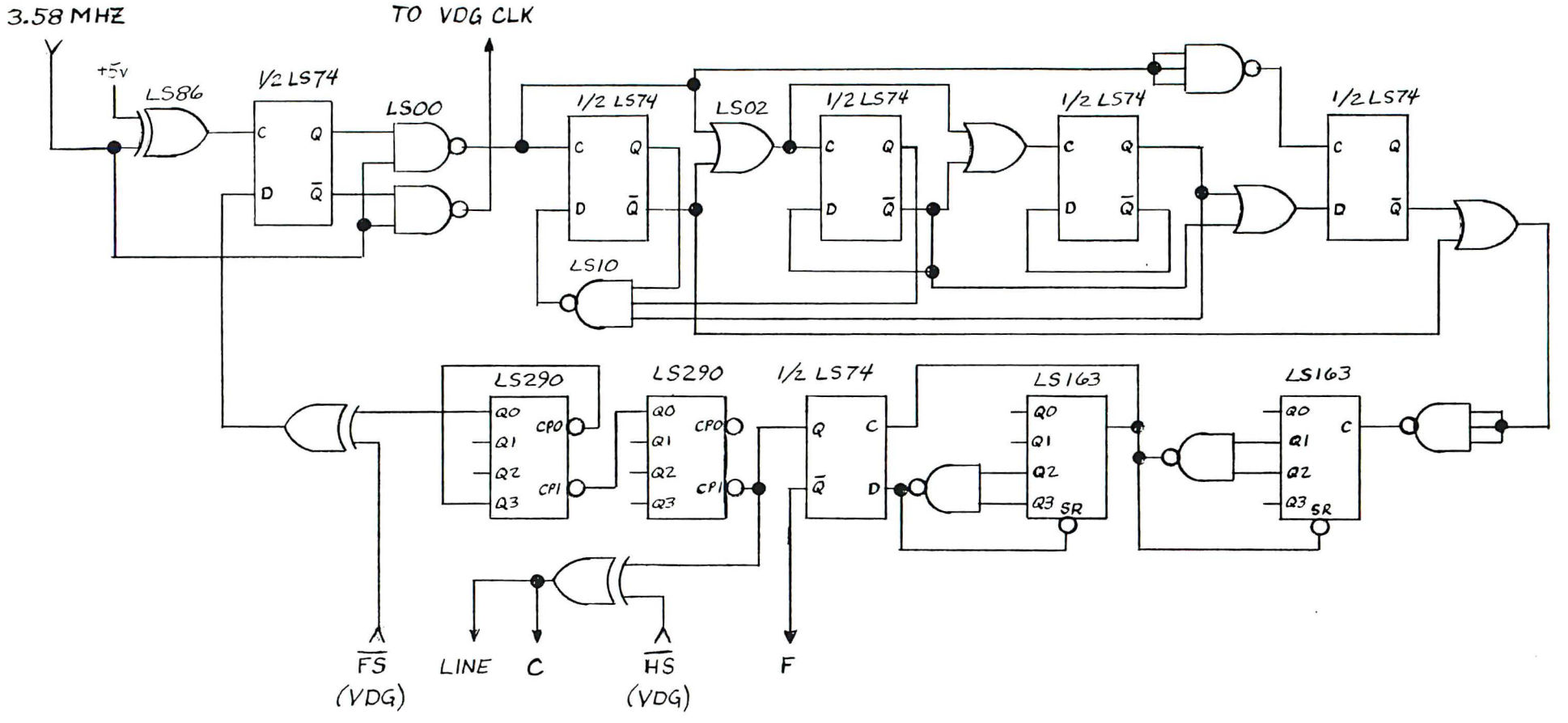


Figure 1. Logic Circuit to Add 100 Blank Lines.

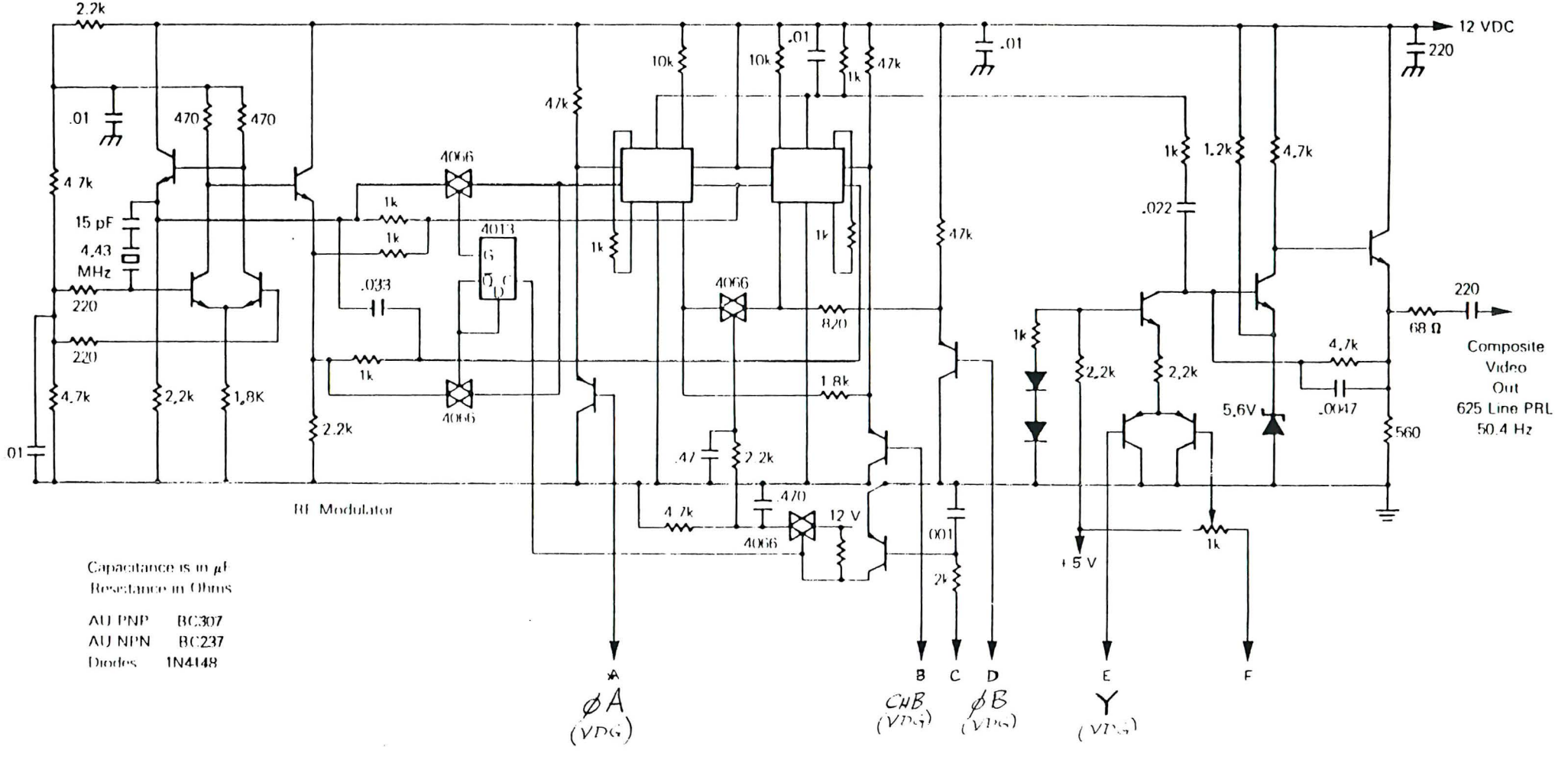


Figure 2. P.A.L. Adapter.

AU PNP BC307
AU NPN BC237
DIODES IN4148

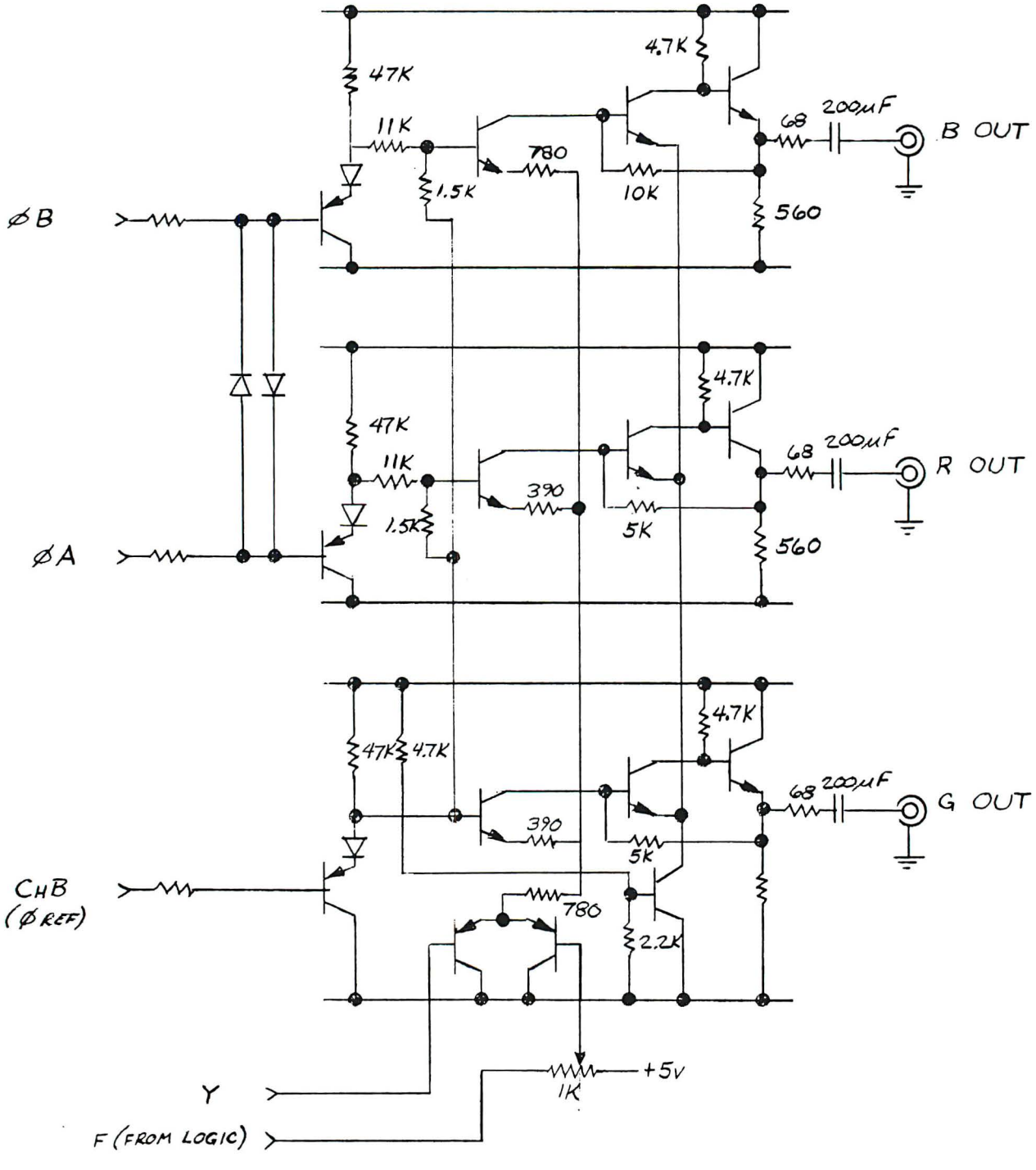


Figure 3. Matrix with Crossfeed and 75 Ohm Outputs for R, G, B Drive From VDG.

Appendix VI

Kit Lists

1.0 COMMON COMPONENTS KIT LIST (KIT 0)

QTY	DESCRIPTION	CPN	REFERENCE DESIGNATION
3	74LS85	351-1697-010	U5, U7, U8
1	74LS30	351-1523-140	U9
1	74LS10	351-1523-230	U10
2	74LS244	351-1841-030	U85, U86
2	74LS00	351-1523-110	U87, U113
2	74LS02	351-1523-220	U98, U120
1	74LS138	351-1526-030	U118
1	74LS32	351-1523-260	U119
10	0.1-μF capacitor	913-3279-200	C56 to C65
1	Terminal blk	367-1599-120	TB1
7	Stand-off, 0.25 in	540-9033-003	-
14	Screw, 0.25 in, 4-40	343-0133-000	-
7	Washer, 0.25 OD	310-0779-030	-
1	Printed circuit board	-	VIDEO-1

2.0 VIDEO COMPONENTS KIT LIST (KIT 1)

QTY	DESCRIPTION	CPN	REFERENCE DESIGNATION
1	74LS374	351-1821-030	U1
2	74LS245	351-1849-020	U2, U117
3	74LS244	351-1841-030	U3, U4, U88
1	74LS42	351-1526-050	U6
1	MC6847	128-0076-001	U11
1	MC1372	128-0076-002	U12
1	74LS00	351-1523-110	U99
1	1 kΩ, 1/4 W, 5%	745-0748-000	R1
1	2 kΩ, 1/4 W, 5%	745-0759-000	R2
1	5.6 kΩ, 1/4 W, 5%	745-0775-000	R3
1	750 Ω, 1/4 W, 5%	745-0744-000	R4
1	75 Ω, 1/4 W, 5%	745-0708-000	R5
2	240 Ω, 1/4 W, 5%	745-0726-000	R6, R7
1	10-kΩ trimmer	382-0012-290	R8
17	0.1-μF capacitor	913-3279-200	C1, C3, C4, C8, C9 to C21
1	47-pF capacitor	913-1098-020	C2
1	56-pF capacitor	913-4003-000	C5
1	0.01-μF capacitor	913-3281-320	C7
1	9- to 35-pF trimmer	917-1225-000	C6
1	0.001-μF capacitor	913-3281-270	C135
1	1-μH coil, adj	242-0447-220	L1
1	Phono jack		J2
1	Bracket, mtg	763-7388-004	-
2	Screw, 0.25 in, 4-40	343-0133-000	-
2	Nut, hex, 4-40	313-0132-000	-

3.0 FUNCTION COMPONENTS KIT LIST (KIT 2)

QTY	DESCRIPTION	CPN	REFERENCE DESIGNATION
1	LM319N	351-1166-010	U89
1	74LS112	351-1525-030	U90
7	74LS374	351-1821-030	U91, U92, U96, U102, U104, U105, U106
4	4051	351-8236-010	U93, U95, U110, U111
5	LF356N	351-1287-040	U94, U97, U109, U130, U131
1	2502	128-0076-003	U100
3	1408	351-1152-010	U101, U107, U108
1	LM340T-15	351-1120-050	U114
1	555	351-1137-020	U115
1	74LS245	351-1849-020	U117
1	74LS00	351-1523-110	U121
1	4053	351-8236-020	U122
1	74LS123	351-1699-020	U123
1	LM318	351-1153-040	U124
1	LM317MP	128-0076-005	U125
1	LM337MP	128-0076-007	U126
2	LM340LAZ-5	128-0076-006	U127, U128
1	LM320LZ-5	128-0076-008	U129
1	2N2222A	352-0661-020	Q1
1	2N2907A	352-0551-010	Q2
1	MRD370	128-0076-004	Q3
3	1N5415	353-6558-010	CR1, CR2, CR3
2	1 kΩ, 1/8 W, 5%	745-1863-490	R9, R41
2	100 Ω, 1/8 W, 5%	745-1863-250	R11, R12
3	10 kΩ, 1/8 W, 5%	745-1863-730	R49, R48, R39
2	2 kΩ, 1/8 W, 5%	745-1863-560	R15, R17
9	3 kΩ, 1/8 W 5%	745-1863-600	R22, R23, R24, R28, R29, R30, R33, R34, R35
1	27 kΩ, 1/8 W, 5%	745-1863-830	R36
1	2.4 kΩ, 1/8 W, 5%	745-1863-580	R46
3	4.7 kΩ, 1/8 W, 5%	745-1863-650	R38, R47, R55
1	36 kΩ, 1/8 W, 5%	745-1863-860	R49
1	150 kΩ, 1/8 W, 5%	745-1864-050	R50
1	300 kΩ, 1/8 W, 5%	745-1864-120	R51
3	1.5 kΩ, 1/8 W, 5%	745-1863-530	R45, R54, R67
10	47 Ω, 1/8 W, 5%	745-1863-170	R58, R59, R60, R61, R62, R63, R64, R65, R66, R67
2	20 Ω, 1/8 W, 5%	745-1863-080	R56, R57
1	120 Ω, 1/8 W, 5%	745-1863-270	R19
1	240 Ω, 1/8 W, 5%	745-1863-340	R13
1	45.3 Ω, 1 W, 1%	747-2178-970	R16
1	2-kΩ trimmer	382-0012-270	R20
4	5-kΩ trimmer	382-0012-280	R21, R25, R31, R14
3	10-kΩ trimmer	382-0012-290	R10, R26, R32
1	20-kΩ trimmer	382-0012-300	R53
1	100-kΩ trimmer	382-0012-330	R37
1	1-MΩ trimmer	382-0012-370	R52
3	1-MΩ network	350-4030-150	R42, R43, R44

4.0 AUXILIARY MEMORY COMPONENTS KIT LIST (KIT 3)

QTY	DESCRIPTION	CPN	REFERENCE DESIGNATION
1	74LS245	351-1849-020	U116
4	74LS138	351-1526-030	U25, U26, U83, U84
1	74LS244	351-1841-030	U103
34	0.1-μF capacitor	913-3279-200	C22 to C55
1	0.1-μH coil	240-2715-000	L2
1	47 μF, 35 V, T	184-9102-890	C66
1	47 μF, 20 V, T	184-9102-190	C67
3	10 μF, 20 V, T	184-9102-170	C68, C73, C74
2	0.01 μF ceramic	913-3279-110	C70, C71
1	15 μF, 20 V, T	184-9086-490	C72
3	15 pF, mica	912-4141-130	C76, C83, C92
3	68 pF, mica	912-4141-330	C79, C86, C95
1	82 pF, mica	912-4141-350	C98
57	0.1 μF, ceramic	913-3279-200	C69, C130, C131, C132, C77, C78, C80, C81, C75, C87, C88, C82, C84, C85, C89, C90, C113, C114, C91, C93, C94, C96, C97, C104, C105, C106, C107, C108, C109, C110, C111, C112, C100, C101, C102, C103, C99, C115, C116, C117, C118, C119, C120, C121, C122, C123, C124, C125, C126, C127, C128, C129, C130, C131, C132, C133, C134
6 ft	Shielded, twisted pair	439-0650-000	-
6 in	Tubing, alum, 0.200 ID	804-3084-022	-
1	Screw, 0.25 in 4-40	343-0133-000	-
1	Nut, hex 4-40	313-0132-000	-

5.0 SOCKET KIT LIST (KIT 4)

QTY	DESCRIPTION	CPN	REFERENCE DESIGNATION
7	8-pin socket	220-0075-010	
12	14-pin socket	220-0075-020	
19	16-pin socket	220-0075-110	
68	18-pin socket	220-0075-090	
17	20-pin socket	220-0075-080	
1	24-pin socket	220-0075-130	
1	40-pin socket	220-0075-150	

Appendix VII

Alphanumeric Software Documentation Package (AIM-65 and VIDEO-1)

A I M - 6 5
V I D E O - 1
ALPHANUMERIC
S O F T W A R E
DOCUMENTATION
P A C K A G E

R I C H
K E T C H A M

6 - 2 - 8 0

-> INTRODUCTION

THIS WRITE-UP IS INTENDED TO GIVE A BRIEF OVERVIEW OF THE VIDEO-1 ALPHA SOFTWARE PACKAGE CALLED "VDG0D" THE INTENT OF THIS PROGRAM IS TO PROVIDE OWNERS OF THE VIDEO-1 BOARD WITH A MEANS OF INCORPORATING THEIR VIDEO PORT(WHILE IN THE ALPHA MODE)INTO THE INSTRUCTION STREAM OF THE AIM-65 MONITOR. THE USER IS REMINDED THAT THIS IS A PRELIMINARY VERSION SO THAT USERS CAN BRING THEIR BOARDS UP AND IT SHOULD NOT BE CONSIDERED A FINAL VERSION.

-> INSTRUCTIONS

THIS SOFTWARE RELEASE DOES NOT PROVIDE AN IDEAL VIDEO DRIVER AS THE EXACT LINKAGE INTO THE MONITOR FOR MANY COMMON VIDEO TERMINAL COMMANDS(I.E.: CURSOR UP,DOWN)ARE YET TO BE CLEARLY DEFINED. AS A RESULT MANY OF THESE ARE NOT INCLUDED AS PART OF THIS RELEASE. THOSE FUNCTIONS INCLUDED ARE INVOKED BY SIMULTANEOUSLY DEPRESSING THE CONTROL KEY("CTRL")AND THE ASSOCIATED COMMAND KEY. A LIST OF COMMANDS AND COMMAND KEYS IS SHOWN BELOW.

M-> CARRIAGE RETURN AND LINE FEED

H-> HOME CURSOR

C-> CLEAR SCREEN& HOME CURSOR

R-> INDIVIDUAL CHAR REVERSE VIDEO

F-> FLIP: WHEN INITIALIZED,THE VIDEO SOFTWARE WILL PROVIDE WHITE CHARS.ON A BLACK BACKGROUND."CTRL F" WILL FLIP THIS TO A BLACK ON WHITE FORMAT. EXECUTING ANOTHER"CTRL F" WILL FLIP IT BACK TO THE ORIGINAL FORMAT

S-> PAGE SWAP: THIS RELEASE PROVIDES 11 PAGES OF STORAGE IN ADDITION TO WHAT IS VISIBLE ON THE TV SCREEN. THE VALID PAGE DESIGNATORS ARE 0 THROUGH 9,A&B WITH PAGE 0 BEING THE ACTIVE PAGE OR THE PAGE VISIBLE ON THE TV. UPON DOING A "CTRL S" ENTER THE DESIGNATOR OF THE PAGE YOU WISH SWAPPED WITH PAGE 0.

Q-> QUIT VIDEO: "CTRL Q" REMOVES THE VIDEO SOFTWARE FROM THE INSTRUCTION STREAM.THE CTRL KEYS WILL NO LONGER BE EXECUTED.

B-> BLAST: THIS FUNCTION DOES A "CTRL Q" IN ADDITION TO PUTTING THE VDG CHIP INTO MAX. GRAPHICS AND CLEARS THE TV SCREEN.

-> INSTALLATION

WE ELECTED TO PROVIDE USERS OF THE VIDEO-1 BOARD WITH A SOURCE LISTING SO THAT THIS PACKAGE CAN BE INSTALLED ON ANY SYSTEM REGARDLESS OF HARDWARE CONFIGURATION. THIS CAN EASILY BE DONE AT ASSEMBLY TIME BY ALTERING THE LOCATION OF THE "SAVE BUFFER"AND PROGRAM ORIGIN. THE LISTING PROVIDED HERE SHOWS THE SOFTWARE CONFIGURED FOR A FULL SYSTEM(THE BUFFER IS LOCATED AT THE TOP END OF USER MEMORY AND THE PROGRAM RESIDES IN THE 2716 EPROM MEMORY AREA). FOR THOSE USERS WHO INTEND TO OPERATE WITH JUST THE 4K OF RAM ON THE AIM-65 THIS BUFFER MIGHT BE LOCATED AT $0FD0. WHATEVER THE CONFIGURATION, THE SAVE BUFFER MUST BE LOCATED IN RAM. THE ACTUAL PROGRAM MAY BE EITHER RAM OR EPROM RESIDENT.

-> NOTES ON USE

TO INSERT THE PRGM INTO THE INSTRUCTION STREAM START EXECUTION AT THE LOCATION LABELED "INITI". IN THE LISTING PROVIDED THIS OCCURS AT $9800

THE SCREEN WILL THEN CLEAR AND THE CURSOR WILL APPEAR AT THE UPPER LEFT HAND CORNER OF THE TV SCREEN.

TO REMOVE THIS SOFTWAE FROM THE INSTRUCTION STREAM EXECUTE A "CTRL Q"

-> SPECIAL NOTES

AS STATED EARLIER IN THIS WRITE-UP THE EXACT LINKAGE FOR MANY FUNCTIONS ARE STILL UNDER STUDY. THE REASON BEING THAT MUCH OF THE SOFTWARE WE ARE ATTEMPING TO LINK WITH IS NOT DOCUMENTED(I.E. ASSEMBLER, BASIC &PL/65)AND THE ACTUAL MECHANICS FOR PROPER OPERATION MUST BE FOUND ON A TRIAL&ERROR BASIS. AS A RESULT, THIS PROGRAM CONTAINS CERTAIN BUGS THE USER SHOULD BE AWARE OF

AT PRESENT, "VDG0D" CONTAINS ONE KNOWN FATAL BUG WHICH WILL CAUSE THE AIM TO "GO TO LUNCH". THIS OCCURS WHEN THE USER ATTEMPTS TO OPERATE THE AIM IN THE SINGLE-STEP MODE THIS OCCURS BECAUSE THIS IS AN INTERRUPT DRIVEN MODE OF OPERATION AND THE PROPER INTERRUPT VECTOR IS NOT ESTABLISHED PRIOR TO THE FIRST INTERRUPT THE MAIN CAUSE OF THIS IS BECAUSE OUR SOFTWARE DOES NOT RESIDE IN A PROTECTED MEMORY AREA A SUITABLE PATCH IS UNDER STUDY AT THIS TIME.

OTHER QUIRKS DO EXIST BUT THEY ARE NOT FATAL IN NATURE. TWO OBVIOUS BUGS THAT ARE KNOWN TO EXIST ARE:

1) THE GAP LENGTH YOU USE WITH YOUR TAPE RECORDER MAY HAVE TO BE INCREASED TO ALLOW FOR THE ADDITIONAL EXECUTION TIME WHEN READING TAPES. UPON ENTRY TO THIS SOFTWARE THE GAP IS AUTOMATICALLY INCREASED TO $40. IT IS RESTORED TO $08 UPON EXECUTION OF A CTRL Q OR B.

2) THIS SOFTWARE DOES NOT REGISTER ANY DELETE KEY ACTIVITY. THE DELETE KEY STILL FUNCTIONS AS USUAL THOUGH.

REMEDIES FOR THESE BUGS ARE UNDER STUDY AT THIS TIME AND HOPEFULLY THEY WILL NOT BE PRESENT IN FUTURE VERSIONS. IF, DURING YOUR USE OF THIS SOFTWARE YOU ENCOUNTER ANY BUGS NOT MENTIONED ABOVE I WOULD LIKE TO BE NOTIFIED AS TO WHAT THEY ARE AND HOW YOU ENCOUNTERED THEM. JUST JOT DOWN THE SITUATION AND SEND IT TO:

RICH KETCHAM
3031 ELAINE DR. N.W.
CEDAR RAPIDS, IOWA
52405

THE REST OF THIS DOCUMENT CONSISTS OF THE SOURCE LISTING, ASSEMBLY LISTING AND A DISASSEMBLY. I WOULD LIKE TO APOL-OGIZED FOR THE DOC-UMENTATION THAT IS PRESENT ON THIS PACKAGE BUT TIME DID NOT ALLOW FOR A THOROUGH JOB.

MANY THANKS TO ALL THOSE WHO HAVE GIVEN ME TONS OF FEEDBACK(INCLUDING MY WIFE DEB), I HOPE IT CONTINUES. HAVE FUN PROGRAMMING THIS BEAST IN AND IN BRINGING IT UP ON YOUR SYSTEM.

"KETCH"

```
OUT=
;-+---+-+-+-+-+-+-+-
;FILE  VDG0D
;
;
;WRITTEN BY:
;RICK KETCHAM
;6-2-80
;
;VIDEO-1 SOFTWARE
;
;
;-+---+-+-+-+-+-+-+-
 PAGE 'DEFINE ZERO P
AGE'
*=$00EC
MAP *=*+2
DUMP *=*+1
REVRS *=*+1
FLAG *=*+1
INCR *=*+1
CURSOR *=*+1
CRTEMP *=*+1
CURSID *=*+1
TEMPID *=*+1
MAP1 *=*+2
 PAGE 'DEFINE LINKS
& PORTS'
PLINT=$9FF8
MODE=$9FFF
DILINK=$A406
TAPSPD=$A409
 PAGE 'DEFINE MONIT
 ADDRES'
READ=$E93C
HEX=$EA7D
PHXY=$EB9E
PLXY=$EBAC
ENTRY=$E182
OUTDIS=$EF05
 PAGE 'ALLOCATE SAVE
 BUFFER'
*=$7FD0
STOR *=*+20
 PAGE 'PROGRAM ORIGI
N'
*=$9800
 PAGE 'TURN VIDEO ON

INITI JSR SWAP
LDA #0
STA MODE
STA CURSOR
STA FLAG
STA REVRS
STA MAP
LDA #$1F
STA CURSID
LDA #$20
STA DUMP
STA TEMPID
LDA #$40
STA TAPSPD
LDA #$80
STA MAP+1
LDA #<TEST
STA DILINK
LDA #>TEST
STA DILINK+1
JSR CLEAR
JSR SWAP
JMP ENTRY
 PAGE 'ACTUAL MONIT
 PATCH'
TEST JSR DISPLA
JSR OUTDIS
RTS
 PAGE 'FULL VERTICAL
 DELAY'
DELAYW PHA
LOOPW LDA PLINT
LSR A
BCS LOOPW
LOOPX LDA PLINT
LSR A
BCC LOOPX
PLA
RTS
 PAGE 'PARTIAL DELAY
'
DELAYV PHA
LOOP1 LDA PLINT
LSR A
BCC LOOP1
PLA
RTS
 PAGE 'CLEAR VIEWING
 PAGE

CLEAR PHA
JSR PHXY
JSR BASE
LDY #0
LDA DUMP
JSR DELAYW
CLEAR1 STA (MAP),Y
INC MAP
BNE CLEAR2
INC MAP+1
CLEAR2 LDX MAP+1
CPX #$82
BNE CLEAR1
JSR BASE
JSR PLXY
PLA
RTS
 PAGE 'ESTAB  ZERO P
AGE RAM'
SWAP PHA
JSR PHXY
LDY #0
SWAP1 LDX MAP,Y
LDA STOR,Y
STA MAP,Y
TXA
STA STOR,Y
INY
CPY #15
BNE SWAP1
JSR PLXY
PLA
RTS
 PAGE 'ALPHA-NU DISP
LAY PCU'
DISPLA PHA
JSR PHXY
JSR SWAP
TAY
CMP #$20
BCS DIS6
JSR CDSTRP
JMP DIS5
DIS6 CMP #$8D
BNE DIS1
AND #$7F
JSR CDSTRP
JMP DIS5
DIS1 CMP #$20
BNE DISA
```

```
TSX
LDA $L07,X
CMP #$E7
BNE DISA
LDA $L06,X
CMP #$F2
BNE DISA
LDA #$09
JSR CDSTRP
JMP DIS5
DISA TYA
LDY TEMPID
STY CRTEMP
AND #$7F
LDY REVRS
BEQ DIS3
CLC
ADC #$80
DIS3 LDY CURSOR
STA (MAP),Y
INY
CPY #32
BNE DIS4
JSR UPDATE
DIS4 STY CURSOR
JSR RESTOR
DIS5 JSR SWAP
JSR PLXY
PLA
RTS
 PAGE 'UPDATE CURSOR
 & PAGE'
UPDATE LDY #0
STY CURSOR
LDA FLAG
BEQ UPD1
JSR SCROLL
JSR CLRCLR
JMP UPD2
UPD1 LDA #32
STA INCR
JSR INCMAP
LDA MAP
CMP #$E0
BNE UPD2
LDA MAP+1
CMP #$81
BNE UPD2
LDA #1
STA FLAG
UPD2 LDY CURSOR
RTS
 PAGE 'EXECUTE CNTL
KEYS
;
;DO WE QUIT ?
;
CDSTRP CMP #$11
BNE CDS6
LDA #$EF
STA CILINK+1
LDA #$05
STA CILINK
LDA #$08
STA TAPSPD
JMP CDSF
;
;DOES CURSOR GO HOME
;
CDS6 CMP #$08
BNE CDS7
JSR GETTMP
LDY #0
STY CURSOR
STY FLAG
JSR BASE
JSR SAVTMP
JSR RESTOR
JMP CDSF
;
;REVERSE VIDEO ?
;
CDS7 CMP #$12
BNE CDS8
LDA REVRS
EOR #1
STA REVRS
JMP CDSF
CDS8 LDY TEMPID
STY CRTEMP
;
;DO WE CLEAR SCREEN?
;
CMP #$03
BNE CDS9
JSR CLEAR
LDA #0
STA FLAG
TAY
STY CURSOR
JSR RESTOR
JMP CDSF
;
;CR&LF ?
;
CDS9 CMP #$0D
BNE CDSA
JSR GETTMP
JSR UPDATE
JSR RESTOR
JMP CDSF
;
;IS IT A PAGE SWAP ?
;
CDSA CMP #$13
BNE CDS00
PAGS JSR READ
JSR HEX
BCS PAGS
CMP #12
BPL PAGS
ASL A
CLC
ADC #$80
STA MAP1+1
LDA #0
STA MAP1
LDA TEMPID
LDY CURSOR
STA (MAP),Y
JSR BASE
LDY #0
JSR DELAYW
PAG1 LDA (MAP),Y
TAX
LDA (MAP1),Y
STA (MAP),Y
TXA
STA (MAP1),Y
CPY #$FF
BEQ PAG2
INY
JMP PAG1
PAG2 INC MAP+1
INC MAP1+1
LDX MAP+1
CPX #$82
BEQ PAG3
LDY #0
BEQ PAG1
PAG3 JSR BASE
LDY #0
STY FLAG
STY CURSOR
JSR RESTOR
JMP CDSF
;
;DO WE FLIP SCREEN ?
;
CDS00 CMP #$06
BNE CDS01
```

```
FLIP LDA DUMP
EOR #$80
STA DUMP
LDA CURSID
EOR #$80
STA CURSID
LDA TEMPID
EOR #$80
STA TEMPID
LDA REVRS
EOR #$01
STA REVRS
LDA #$00
STA MAP1
LDA #$80
STA MAP1+1
LDY #0
JSR DELAYW
FLIP1 LDA (MAP1),Y
EOR #$80
STA (MAP1),Y
INC MAP1
BNE FLIP2
INC MAP1+1
FLIP2 LDA MAP1+1
CMP #$82
BNE FLIP1
JMP CDSF
;
;DO WE BLAST SCREEN?
;
CDS01 CMP #$02
BNE CDSF
BLAST LDA #$FF
STA MODE
LDA #$80
STA MAP+1
LDA #$00
STA MAP
TAY
BLAST1 STA (MAP),Y
INC MAP
BNE BLAST2
INC MAP+1
BLAST2 LDX MAP+1
CPX #$98
BNE BLAST1
LDA #<OUTDIS
STA DILINK
LDA #>OUTDIS
STA DILINK+1
LDA #$08
STA TAPSPD
JMP CDSF
CDSF RTS
.PAGE 'RESTORE CHARA
CTER'
GETTMP LDY CURSOR
LDA CRTEMP
STA (MAP),Y
RTS
.PAGE 'GET CHARACTER
'
SAVTMP LDY CURSOR
LDA (MAP),Y
STA CRTEMP
RTS
.PAGE 'RESTORE CURSO
R'
RESTOR LDY CURSOR
LDA CURSID
STA (MAP),Y
RTS
.PAGE 'SCROLL PAGE O
NE LINE'
SCROLL PHA
JSR PHXY
JSR BASE
LDA #1
STA INCR
JSR DELAYW
SCR1 LDY #32
LDA (MAP),Y
LDY #0
STA (MAP),Y
JSR INCMAP
LDA MAP
CMP #$E0
BNE SCR1
LDA MAP+1
CMP #$81
BNE SCR1
JSR PLXY
PLA
RTS
.PAGE 'CLEAR BOTTOM
LINE'
LINCLR PHA
JSR PHXY
LDY CURSOR
LDA DUMP
LIN1 STA (MAP),Y
INY
CPY #32
BNE LIN1
JSR PLXY
PLA
RTS
.PAGE 'INCR. MAP BY
"INCR"'
INCMAP PHA
LDA MAP
CLC
ADC INCR
STA MAP
LDA #0
ADC MAP+1
STA MAP+1
PLA
RTS
.PAGE 'SET TO UPPER
LEFT'
BASE LDA #0
STA MAP
LDA #$80
STA MAP+1
RTS
.END
```

```
==0000
;-+---+-+-+-+-+-+-
;FILE  VDG80D
;
;
;WRITTEN BY:
;RIC- KETCHAM
;6-2-80
;
;VIDEO-1 SOFTWARE
;
;
;-+---+-+-+-+-+-+-
--------------------
DEFINE ZERO PAGE

==0000
        *=$00EC
==00EC  MAP
        *=*+2
==00EE  DUMP
        *=*+1
==00EF  REVRS
        *=*+1
==00F0  FLAG
        *=*+1
==00F1  INCR
        *=*+1
==00F2  CURSOR
        *=*+1
==00F3  CRTEMP
        *=*+1
==00F4  CURSID
        *=*+1
==00F5  TEMPID
        *=*+1
==00F6  MAP1
        *=*+2
--------------------
DEFINE LINKS & PORTS

==00F8  PLINT=$9FF8

==00F8  MODE=$9FFF

==00F8  DILINK=$A406

==00F8  TAPSPD=$A409

--------------------
DEFINE MONIT. ADDRES

==00F8  READ=$E93C

==00F8  HEX=$EA7D

==00F8  PHXY=$EB9E

==00F8  PLXY=$EBAC

==00F8  ENTRY=$E182

==00F8  OUTDIS=$EF05

--------------------
ALLOCATE SAVE BUFFER

==00F8
        *=$7FD0
==7FD0  STOR
        *=*+20
--------------------
PROGRAM ORIGIN

==7FE4
        *=$9800
--------------------
TURN VIDEO ON

==9800  INITI
207098  JSR SWAP
A900    LDA #0
8DFF9F  STA MODE
85F2    STA CURSOR
85F0    STA FLAG
85EF    STA REVRS
85EC    STA MAP
==9810
A91F    LDA #$1F
85F4    STA CURSID
A920    LDA #$20
85EE    STA DUMP
85F5    STA TEMPID
A940    LDA #$40
8D09A4  STA TAPSPD
A980    LDA #$80
==9821
85ED    STA MAP+1
A936    LDA #<TEST
8D06A4  STA DILINK
A998    LDA #>TEST
8D07A4  STA DILINK+1
205598  JSR CLEAR
207098  JSR SWAP
==9832
4C82E1  JMP ENTRY
--------------------
ACTUAL MONIT  PATCH

==9836  TEST
209598  JSR DISPLA
2005EF  JSR OUTDIS
60      RTS
--------------------
FULL VERTICAL DELAY

==983D  DELAYW
48      PHA
==983E  LOOPW
ADF89F  LDA PLINT
4A      LSR A
B0FA    BCS LOOPW
==9844  LOOPX
ADF89F  LDA PLINT
4A      LSR A
90FA    BCC LOOPX
68      PLA
60      RTS
--------------------
PARTIAL DELAY

==984C  DELAYV
48      PHA
==984D  LOOP1
ADF89F  LDA PLINT
4A      LSR A,
90FA    BCC LOOP1
68      PLA
60      RTS
```

```
---------------------
CLEAR VIEWING PAGE

==98E5 CLEAR
48     PHA
209EEB JSR PHXY
20AF9A JSR BASE
A000   LDY #0
A5EE   LDA DUMP
203D98 JSR DELAYW
==98ED CLEAR1
91EC   STA (MAP),Y
E6EC   INC MAP
D002   BNE CLEAR2
E6ED   INC MAP+1
==98EB CLEAR2
A6ED   LDX MAP+1
E082   CPX #$82
D0F2   BNE CLEAR1
20AF9A JSR BASE
20ACEB JSR PLXY
68     PLA
60     RTS
---------------------
ESTAB  ZERO PAGE RAM

==98F9 SWAP
48     PHA
209EEB JSR PHXY
A000   LDY #0
==98FF SWAP1
B6EC   LDX MAP,Y
B9D07F LDA STOR,Y
99EC00 STA MAP,Y
8A     TXA
99D07F STA STOR,Y
C8     INY
C00F   CPY #15
D0EF   BNE SWAP1
==9890
20ACEB JSR PLXY
68     PLA
60     RTS
---------------------
ALPHA-NU DISPLAY ROU

==9895 DISPLA
48     PHA
209EEB JSR PHXY
207998 JSR SWAP
A8     TAY
C920   CMP #$20
B006   BCS DIS6
202099 JSR CDSTRP
4CED98 JMP DIS5
==98A7 DIS6
C98D   CMP #$8D
D008   BNE DIS1
297F   AND #$7F
202099 JSR CDSTRP
4CED98 JMP DIS5
==98B3 DIS1
C920   CMP #$20
D017   BNE DISA
BA     TSX
BD0701 LDA $107,X
C9E7   CMP #$E7
D00F   BNE DISA
BD0601 LDA $106,X
C9F2   CMP #$F2
==98C4
D008   BNE DISA
A909   LDA #$09
202099 JSR CDSTRP
4CED98 JMP DIS5
==98CE DISA
98     TYA
A4F5   LDY TEMPID
84F3   STY CRTEMP
297F   AND #$7F
A4EF   LDY REVRS
F003   BEQ DIS3
18     CLC
6980   ADC #$80
==98DC DIS3
A4F2   LDY CURSOR
91EC   STA (MAP),Y
C8     INY
C020   CPY #32
D003   BNE DIS4
20F598 JSR UPDATE
==98E8 DIS4
84F2   STY CURSOR
205A9A JSR RESTOR
==98ED DIS5
207998 JSR SWAP
20ACEB JSR PLXY
68     PLA
60     RTS
---------------------
UPDATE CURSOR & PAGE

==98F5 UPDATE
A000   LDY #0
84F2   STY CURSOR
A5F0   LDA FLAG
F009   BEQ UPD1
20613A JSR SCROLL
208B9A JSR LINCLR
4C1D99 JMP UPD2
==9906 UPD1
A920   LDA #32
85F1   STA INCR
209F9A JSR INCMAP
A5EC   LDA MAP
C9E0   CMP #$E0
D00A   BNE UPD2
A5ED   LDA MAP+1
C981   CMP #$81
==9917
D004   BNE UPD2
A901   LDA #1
85F0   STA FLAG
==991D UPD2
A4F2   LDY CURSOR
60     RTS
---------------------
EXECUTE CNTL KEYS

;
;DO WE QUIT ?
;
==9920 CDSTRP
C911   CMP #$11
D012   BNE CDS6
A9EF   LDA #$EF
8D07A4 STA DILINK+1
A905   LDA #$05
8D06A4 STA DILINK
A908   LDA #$08
==9930
8D09A4 STA TAPSPD
4C4B9A JMP CDSF
```

```
;
;DOES CURSOR GO HOME
;
==99C8 CD56
C908    CMP #$08
D015    BNE CD57
204C9A  JSR GETTMP
A000    LDY #0
84F2    STY CURSOR
84F0    STY FLAG
20AF9A  JSR BASE
==9946
2053AA  JSR SAVTMP
205A9A  JSR RESTOR
4C4B9A  JMP CD5F
;
;REVERSE VIDEO ?
;
==994F CD57
C912    CMP #$12
D009    BNE CD58
A5EF    LDA REVRS
4901    EOR #1
85EF    STA REVRS
4C4B9A  JMP CD5F
==9959 CD58
A4F5    LDY TEMPID
84F3    STY CRTEMP
;
;DO WE CLEAR SCREEN?
;
C903    CMP #$03
D010    BNE CD59
2055A8  JSR CLEAR
A900    LDA #0
85F0    STA FLAG
A8      TAY
==9967
84F2    STY CURSOR
205A9A  JSR RESTOR
4C4B9A  JMP CD5F
;
;CR&LF ?
;
==9974 CD59
C90D    CMP #$0D
D00C    BNE CD5A
204C9A  JSR GETTMP
20F5A3  JSR UPDATE
205A9A  JSR RESTOR
4C4B9A  JMP CD5F
==9984
;
;IS IT A PAGE SWAP ?
;
==9984 CD5A
C913    CMP #$13
D053    BNE CD500
==9988 PAG5
203CE9  JSR READ
207DEA  JSR HEX
B0F8    BCS PAG5
C90C    CMP #12
10F4    BPL PAG5
0A      ASL A
18      CLC
6980    ADC #$80
==9998
85F7    STA MAP1+1
A900    LDA #0
85F6    STA MAP1
A5F5    LDA TEMPID
A4F2    LDY CURSOR
91EC    STA (MAP),Y
20AF9A  JSR BASE
A000    LDY #0
==99A8
203D96  JSR DELAYW
==99AC PAG1
B1EC    LDA (MAP),Y
AA      TAX
B1F6    LDA (MAP1),Y
91EC    STA (MAP),Y
8A      TXA
91F6    STA (MAP1),Y
C0FF    CPY #$FF
F004    BEQ PAG2
C8      INY
4CAC99  JMP PAG1
==99BE PAG2
E6ED    INC MAP+1
E6F7    INC MAP1+1
A6ED    LDX MAP+1
E082    CPX #$82
F004    BEQ PAG3
A000    LDY #0
F0E0    BEQ PAG1
==99CC PAG3
20AF9A  JSR BASE
A000    LDY #0
84F0    STY FLAG
84F2    STY CURSOR
205A9A  JSR RESTOR
4C4B9A  JMP CD5F
;
;DO WE FLIP SCREEN ?
;
==99DB CD500
C906    CMP #$06
D03A    BNE CD501
==99DF FLIP
A5EE    LDA DUMP
4980    EOR #$80
85EE    STA DUMP
A5F4    LDA CURSID
4980    EOR #$80
85F4    STA CURSID
A5F5    LDA TEMPID
4980    EOR #$80
==99EF
85F5    STA TEMPID
A5EF    LDA REVRS
4901    EOR #$01
85EF    STA REVRS
A900    LDA #$00
85F6    STA MAP1
A980    LDA #$80
85F7    STA MAP1+1
==99FF
A000    LDY #0
203D96  JSR DELAYW
==9A04 FLIP1
B1F6    LDA (MAP1),Y
4980    EOR #$80
91F6    STA (MAP1),Y
E6F6    INC MAP1
D002    BNE FLIP2
E6F7    INC MAP1+1
==9A10 FLIP2
A5F7    LDA MAP1+1
C982    CMP #$82
D0EE    BNE FLIP1
4C4B9A  JMP CD5F
;
;DO WE BLAST SCREEN?
;
==9A19 CD501
C902    CMP #$02
D02E    BNE CD5F
==9A1D BLAST
A9FF    LDA #$FF
8DFF9F  STA MODE
A980    LDA #$80
85ED    STA MAP+1
A900    LDA #$00
85EC    STA MAP
A8      TAY
```

```
==9A??  BLAST1
91EC    STA (MAP),Y
E6EC    INC MAP
D002    BNE BLAST2
E6ED    INC MAP+1
==9A??  BLAST2
A6ED    LDX MAP+1
E098    CPX #$98
D0F2    BNE BLAST1
A905    LDA #<OUTDIS
8D06??  STA DILINK
A9EF    LDA #>OUTDIS
8D07??  STA DILINK+1
==9A??
A908    LDA #$08
8D09??  STA TAPSPD
4C4B??  JMP CDSF
==9A??  CDSF
60      RTS

---------------------
RESTORE CHARACTER

==9A??  GETTMP
A4F2    LDY CURSOR
A5??    LDA CRTEMP
91EC    STA (MAP),Y
60      RTS

---------------------
GET CHARACTER

==9A??  GETMAP
A4F2    LDY CURSOR
B1EC    LDA (MAP),Y
85??    STA CRTEMP
60      RTS

---------------------
RESTORE CURSOR

==9A??  RESTOR
A4F2    LDY CURSOR
A5F4    LDA CURSOR+1
91EC    STA (MAP),Y
60      RTS
```

```
---------------------
SCROLL PAGE ONE LINE

==9A??  SCROLL
48      PHA
209E??  JSR PHXY
20AF??  JSR BASE
A901    LDA #1
85F1    STA INCR
203D??  JSR DELAYW
==9A??  SCR1
A020    LDY #32
B1EC    LDA (MAP),Y
A000    LDY #0
91EC    STA (MAP),Y
209F??  JSR INCMAP
A5EC    LDA MAP
C9E0    CMP #$E0
D0EF    BNE SCR1
==9A??
A5ED    LDA MAP+1
C981    CMP #$81
D0E9    BNE SCR1
20AC??  JSR PLXY
68      PLA
60      RTS

---------------
CLEAR BOTTOM LINE

==9A??  CLRLP
48      PHA
20??    JSR PH.Y
A4F2    LDY CURSOR
A5??    LDA CRTMP
==9A??  CLR2
91EC    STA (MAP),Y
C8      INY
C020    CPY #32
D0??    BNE CLR2
20A???  JSR PLY
68      PLA
60      RTS
```

```
---------------------
INCR  MAP BY "INCR"

==9A??  INCMAP
48      PHA
A5EC    LDA MAP
18      CLC
65F1    ADC INCR
85EC    STA MAP
A900    LDA #0
65ED    ADC MAP+1
85ED    STA MAP+1
68      PLA
60      RTS
---------------------
SET TO UPPER LEFT

==9A??  BASE
A900    LDA #0
85EC    STA MAP
A980    LDA #$80
85ED    STA MAP+1
60      RTS
        END
 ERRORS= 0000
```

ROCKWELL AIM 65

<K>*=9800

```
9800  20 JSR 9879
9803  A9 LDA #00
9805  8D STA 9FFF
9808  85 STA F2
980A  85 STA F0
980C  85 STA EF
980E  85 STA EC
9810  A9 LDA #1F
9812  85 STA F4
9814  A9 LDA #20
9816  85 STA EE
9818  85 STA F5
981A  A9 LDA #40
981C  8D STA A409
981F  A9 LDA #80
9821  85 STA ED
9823  A9 LDA #36
9825  8D STA A406
9828  A9 LDA #98
982A  8D STA A407
982D  20 JSR 9855
9830  20 JSR 9879
9833  4C JMP E182
9836  20 JSR 9895
9839  20 JSR EF05
983C  60 RTS
983D  48 PHA
983E  AD LDA 9FF3
9841  4A LSR  A
9842  B0 BCS 983E
9844  AD LDA 9FF8
9847  4A LSR  A
9848  90 BCC 9844
984A  68 PLA
984B  60 RTS
984C  48 PHA
984D  AD LDA 9FF8
9850  4A LSR  A
9851  90 BCC 984D
9853  68 PLA
9854  60 RTS
9855  48 PHA
9856  20 JSR EB9E
9859  20 JSR 9AAF
985C  A0 LDY #00
985E  A5 LDA EE
9860  20 JSR [illegible]
9863  91 STA (EC),Y
9865  E6 INC EC
9867  D0 BNE [illegible]
9869  E6 INC ED
986B  A5 LDA ED
986D  C9 CMP #81
986F  D0 BNE 985E
9871  20 JSR 9AAF
9874  20 JSR EBAC
9877  68 PLA
9878  60 RTS
9879  48 PHA
987A  20 JSR EB9E
987D  A0 LDY #00
987F  B6 LDX EC,Y
9881  B9 LDA 7FD0,Y
9884  99 STA 00EC,Y
9887  8A TXA
9888  99 STA 7FD0,Y
988B  C8 INY
988C  C0 CPY #0F
988E  D0 BNE 987F
9890  20 JSR EBAC
9893  68 PLA
9894  60 RTS
9895  48 PHA
9896  20 JSR EB9E
9899  20 JSR 9879
989C  A8 TAY
989D  C9 CMP #20
989F  B0 BCS 98A7
98A1  20 JSR 9920
98A4  4C JMP 98ED
98A7  C9 CMP #8D
98A9  D0 BNE 98B3
98AB  29 AND #7F
98AD  20 JSR 9920
98B0  4C JMP 98ED
98B3  C9 CMP #20
98B5  D0 BNE 98CE
98B7  BA TSX
98B8  BD LDA 0107,X
98BB  C9 CMP #E7
98BD  D0 BNE 98CE
98BF  BD LDA 0106,X
98C2  C9 CMP #F2
98C4  D0 BNE 98CE
98C6  A9 LDA #09
98C8  20 JSR 9920
98CB  4C JMP 98ED
98CE  98 TYA
98CF  A4 LDY F5
98D1  84 STY F3
98D3  29 AND #7F
98D5  A4 LDY EF
98D7  F0 BEQ 98DC
98D9  18 CLC
98DA  69 ADC #80
98DC  A4 LDY F2
98DE  91 STA (EC),Y
98E0  C8 INY
98E1  C0 CPY #20
98E3  D0 BNE 98E8
98E5  20 JSR 98F5
98E8  84 STY F2
98EA  20 JSR 9A5A
98ED  20 JSR 9879
98F0  20 JSR EBAC
98F3  68 PLA
98F4  60 RTS
98F5  A0 LDY #00
98F7  84 STY F2
98F9  A5 LDA F0
98FB  F0 BEQ 9906
98FD  20 JSR 9A61
9900  20 JSR 9A8B
9903  4C JMP 991D
9906  A9 LDA #20
9908  85 STA F1
990A  20 JSR 9A9F
990D  A5 LDA EC
990F  C9 CMP #E0
9911  D0 BNE 991D
9913  A5 LDA ED
9915  C9 CMP #81
9917  D0 BNE 991D
9919  A9 LDA #01
991B  85 STA F0
991D  A4 LDY F2
991F  60 RTS
9920  C9 CMP #11
9922  D0 BNE 9936
9924  A9 LDA #EF
9926  8D STA A407
9929  A9 LDA #05
992B  8D STA A406
992E  A9 LDA #08
9930  8D STA A409
9933  4C JMP 9A4B
9936  C9 CMP #08
9938  D0 BNE 994F
993A  20 JSR 9A4C
993D  A0 LDY #00
993F  84 STY F2
9941  84 STY F0
9943  20 JSR 9AAF
9946  20 JSR 9A53
9949  20 JSR 9A5A
994C  4C JMP 9A4B
994F  C9 CMP #12
9951  D0 BNE 995C
9953  A5 LDA EF
9955  49 EOR #01
9957  85 STA EF
9959  4C JMP 9A4B
995C  A4 LDY F5
995E  84 STY F3
9960  C9 CMP #03
9962  D0 BNE 9974
9964  20 JSR 9855
9967  A9 LDA #00
9969  85 STA F0
996B  A8 TAY
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9961  84 STY F2
9963  20 JSR 9A5A
9972  4C JMP 9A4B
9974  C9 CMP #0D
9976  D0 BNE 9984
9978  20 JSR 9A4C
997B  20 JSR 98F5
997E  20 JSR 9A5A
9981  4C JMP 9A4B
9984  C9 CMP #13
9986  D0 BNE 99DB
9988  20 JSR E93C
998B  20 JSR EA7D
998E  B0 BCS 9988
9990  C9 CMP #0C
9992  10 BPL 9988
9994  0A ASL  A
9995  18 CLC
9996  69 ADC #80
9998  85 STA F7
999A  A9 LDA #00
999C  85 STA F6
999E  A5 LDA F5
99A0  A4 LDY F2
99A2  91 STA (EC),Y
99A4  20 JSR 9AAF
99A7  A0 LDY #00
99A9  20 JSR 983D
99AC  B1 LDA (EC),Y
99AE  AA TAX
99AF  B1 LDA (F6),Y
99B2  91 STA (EC),Y
99B4  8A TXA
99B5  91 STA (F6),Y
99B7  C0 CPY #FF
99B9  F0 BEQ 99BE
99BB  C8 INY
99BC  4C JMP 99AC
99BF  E6 INC ED
99C1  E6 INC F7
99C3  A6 LDX ED
99C5  E0 CPX #82
99C7  F0 BEQ 99CC
99C9  A0 LDY #00
99CB  F0 BEQ 99AC
99CD  20 JSR 9AAF
99D0  A0 LDY #00
99D2  84 STY F0
99D4  84 STY F2
99D6  20 JSR 9A5A
99D9  4C JMP 9A4B
99DC  C9 CMP #06
99DE  D0 BNE 9A13
99E0  A5 LDA EE
99E2  49 EOR #80
99E4  85 STA EE
99E6  A5 LDA F4
99E8  49 EOR #80
99EA  85 STA F4
99EC  A5 LDA F5
99EE  49 EOR #80
99F0  85 STA F5
99F2  A5 LDA EF
99F4  49 EOR #01
99F6  85 STA EF
99F8  A9 LDA #00
99FA  85 STA F6
99FC  A9 LDA #80
99FE  85 STA F7
9A00  A0 LDY #00
9A02  20 JSR 983D
9A05  B1 LDA (F6),Y
9A07  49 EOR #80
9A09  91 STA (F6),Y
9A0B  E6 INC F6
9A0D  D0 BNE 9A10
9A0F  E6 INC F7
9A11  A5 LDA F7
9A13  C9 CMP #82
9A15  D0 BNE 9A04
9A17  4C JMP 9A4B
9A1A  C9 CMP #02
9A1C  D0 BNE 9A4B
9A1E  A9 LDA #FF
9A20  8D STA 9FFF
9A23  A9 LDA #80
9A25  85 STA ED
9A27  A9 LDA #00
9A29  85 STA EC
9A2B  A8 TAY
9A2C  91 STA (EC),Y
9A2E  E6 INC EC
9A30  D0 BNE 9A33
9A32  E6 INC ED
9A34  A6 LDX ED
9A36  E0 CPX #98
9A38  D0 BNE 9A2B
9A3A  A9 LDA #05
9A3C  8D STA A406
9A3F  A9 LDA #EF
9A41  8D STA A407
9A44  A9 LDA #08
9A46  8D STA A409
9A49  4C JMP 9A4B
9A4C  60 RTS
9A4D  A4 LDY F2
9A4F  A5 LDA F4
9A51  91 STA (EC),Y
9A53  60 RTS
9A54  A4 LDY F2
9A56  A5 LDA F4
9A58  91 STA (EC),Y
9A5A  60 RTS
9A5B  48 PHA
9A5C  20 JSR EB9E
9A5F  20 JSR 9AAF
9A62  A9 LDA #01
9A64  85 STA F1
9A66  20 JSR 983D
9A69  A0 LDY #20
9A6B  B1 LDA (EC),Y
9A6D  A0 LDY #00
9A6F  91 STA (EC),Y
9A71  20 JSR 9A9F
9A74  A5 LDA EC
9A76  C9 CMP #E0
9A78  D0 BNE 9A6F
9A7A  A5 LDA ED
9A7C  C9 CMP #81
9A7E  D0 BNE 9A6F
9A80  20 JSR EBAC
9A83  68 PLA
9A84  60 RTS
9A85  48 PHA
9A86  20 JSR EB9E
9A89  A4 LDY F2
9A8B  A5 LDA EE
9A8D  91 STA (EC),Y
9A8F  C8 INY
9A90  C0 CPY #20
9A92  D0 BNE 9A93
9A94  20 JSR EBAC
9A97  68 PLA
9A98  60 RTS
9A99  48 PHA
9A9A  A5 LDA EC
9A9C  18 CLC
9A9D  65 ADC F1
9A9F  85 STA EC
9AA1  A9 LDA #00
9AA3  65 ADC ED
9AA5  85 STA ED
9AA7  68 PLA
9AA8  60 RTS
9AA9  A5 LDA #20
9AAB  85 STA EE
9AAD  A9 LDA #80
9AAF  85 STA ED
9AB1  60 RTS
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